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NAVAL POSTGRADUATE SCHOOL Monterey, California



THESIS

L767

THE DESIGN AND IMPLEMENTATION OF A POSITION MEASURING SYSTEM FOR A REMOTELY CONTROLLED VIDEO CAMERA

bу

Peter D. Lloyd

June 1989

Thesis Advisor: Co-Advisor:

Alfred W. Cooper Hal A. Titus

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a Report Security Classification Unclassified	1b Restrictive Markings		
a Security Classification Authority	3 Distribution Availability of Report		
b Declassification Downgrading Schedule	Approved for public release;		
Performing Organization Report Number(s)	5 Monitoring Organization Report Num	nber(s)	
a Name of Performing Organization 6b Office Symbol (if applicable) 62	7a Name of Monitoring Organization Naval Postgraduate School		
Address (city, state, and ZIP code) 1 CA 93943-5000	7b Address (city, state, and ZIP code) Monterey, CA 93943-5000		
Name of Funding Sponsoring Organization 8b Office Symbol (if applicable)	9 Procurement Instrument Identification	Number	
Address (city, state, and ZIP code)	10 Source of Funding Numbers		
	Program Element No Project No Ta		
Title (include security classification) THE DESIGN AND IMPLE OR A REMOTELY CONTROLLED VIDEO CAMERA	MENTATION OF A POSITION	MEASURING SYSTEM	
Personal Author(s) Peter D. Lloyd			
3a Type of Report 13b Time Covered From To	14 Date of Report (year, month, day) June 1989	15 Page Count 133	
Supplementary Notation The views expressed in this thesis are the tion of the Department of Defense or the U.S. Government.	ose of the author and do not refle	ect the official policy or po-	
Abstract (continue on reverse if necessary and identify by block number) A position measuring system for a remotely controlled vide e used with the modified Advance Development Model of th (RSTD) in use at the Naval Postgraduate School. The video cata from the IRSTD to develop a background data base that thms. The measurement system uses two Hewlett Packard 1C68705U3 microprocessors and two digital display devices ngles to an operator at a remote location. The azimuth controlled videously and the elevation can be measured over 24° with a system yet of the backlash in the gears between the	e AN, SAR-8 Infrared Search and data collected by the camera will be t will be used in the development HEDS-6000 incremental optical to measure and present the camera and be measured over a range of resolution of $\pm 0.138^{\circ}$. The resolution	EVM, optical shaft encoder, The camera is intended to Target Designation System e correlated with the infrared nt of signal processing algo- l encoders, two Motorola lera's azimuth and elevation of 360° with a resolution of ution is limited primarily by	
Distribution Availability of Abstract unclassified unlimited same as report DTIC users a Name of Responsible Individual	21 Abstract Security Classification Unclassified 22b Telephone (include Area code)	22c Office Symbol	
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The Design and Implementation of a Position Measuring System for a Remotely Controlled Video Camera

by

Peter D. Lloyd Captain, United States Marine Corps B.S., United States Naval Academy, 1979

Submitted in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL June 1989

ABSTRACT

A position measuring system for a remotely controlled video camera was designed and built. The camera is intended to be used with the modified Advance Development Model of the AN/SAR-8 Infrared Search and Target Designation System (IRSTD) in use at the Naval Postgraduate School. The video data collected by the camera will be correlated with the infrared data from the IRSTD to develop a background data base that will be used in the developement of signal processing algorithms.

The measurement system uses two Hewlett Packard HEDS-6000 incremental optical encoders, two Motorola MC68705U3 microprocessors and two digital display devices to measure and present the camera's azimuth and elevation angles to an operator at a remote location. The azimuth can be measured over a range of 360° with a resolution of ± 0.0213 ° and the elevation can be measured over 24° with a resolution of ± 0.138 °. The resolution is limited primarily by hysteresis, which is due to the backlash in the gears between the transducers and the axes of interest.

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THESIS DISCLAIMER

The reader is cautioned that computer programs developed in this research may not have been exercised for all cases of interest. While every effort has been made, within the time available, to ensure that the programs are free of computational and logic errors, they cannot be considered validated. Any application of these programs without additional verification is at the risk of the user.

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ACKNOWLEDGEMENTS

This thesis is prepared in conjunction with research sponsored in part by the Naval Sea Systems Command, PMS-421, and by the Naval Postgraduate School.

I would like to take a moment to thank the following people who have offered so much and so generously as I have undertaken this project:

My parents who have always helped me through the hard times.

Professor A. W. Cooper for his confidence and insight.

Professor Hal Titus for his constant encouragement, guidance and tremendous sense of humor which made even the difficult times enjoyable.

John Glenn, Jerry Lentz and Eric Moore for their continued technical assistance.

ET2 Akerson for his dedicated work in designing and building the printed circuit boards.

George Jaksha for his expert advice and work in modifying the camera servo mechanism.

I offer my sincere thanks to my fellow officers and students, especially my good friends Capt Steve Spehn and CPT Ken Cockerham for their friendship and thoughtful suggestions.

Finally, I offer my thanks and love to my dear wife, Ellen, who has given so very much in the past two years.

I. INTRODUCTION

A. BACKGROUND

The old saying that "every solution breeds new problems", while somewhat pessimistic, quite often rings true in today's increasingly technical world. One such example is the use of infrared (IR) sensors for the detection, tracking and/or identification of targets in a combat environment. IR sensors are ideally suited for use on today's battlefield. They are passive, i.e., they do not need to emit energy in order to detect the presence of potential targets. This allows them to operate during times of emission control when many other target detection systems are useless. They have the ability to "see through" many forms of camouflage and concealment, dust, clouds, smoke, etc., that might otherwise afford an enemy target a safe haven. Additionally, because almost everything on today's battlefield generates some degree of infrared energy, IR sensors can be used to locate and identify a wide variety of targets.

The extent to which a particular IR sensor is useful depends primarily on its ability to detect and identify targets reliably and accurately. Detection of the target is primarily a function of the IR sensor's sensitivity. The classification of a received IR signal as a potential target or as background noise, while still dependant on the sensitivity of the sensors, is primarily a function of the quality of the signal processing algorithms being used to process the received signals. In addition to being reliable these algorithms must be able to process the received signals in "real time" if the system is to be an effective weapons system.

Creation of a background data base that can be used to test some of these algorithms has been one of the tasks being performed by the Naval Academic Center for Infrared Technology (NACIT) located at the Naval Postgraduate School (NPS). The Advanced Development Model (ADM) of the AN/SAR-8 was sent to the NACIT in January of 1984 from the Naval Surface Weapons Center (NSWC) at Dahlgren, Virginia. The ADM was modified, calibrated and placed in service at NPS in December, 1987. The modified version of the ADM, the Infrared Search and Target Designation (IRSTD) System, is currently operational at NPS. [Ref. 1: pp. 8-12]

One way to enhance the usefulness of the IR data being collected at NPS would be to collect video data concurrently with the IR data. A video image of a portion of the horizon would permit visual identification of IR sources in that region. This additional

tional information could be an aid in the development of the signal processing algorithms for the IRSTD. Accordingly, a decision to proceed with video data collection was made by NACIT, and a camera system was purchased. Components of the system include;

- RCA (TC1005/01), Closed circuit video camera.
- PELCO (AI700), Automatic iris servo.
- PELCO (F1.5X), 1.5 times range extender.
- PELCO (MLZ6DT), Desk top lens remote control module.
- PELCO (PT1250DC), Heavy duty Pan/Tilt servo.
- PELCO (MPTV1510DT), Pan/Tilt remote control unit.
- Panasonic (WV-5410), Video Monitor.

In Ref. 1 Ayers describes the IRSTD's detectors:

The IR detectors consist of two vertical arrays of sensing elements in the focal plane of the Schmidt telescope. The telescope is rotated so as to sweep the image across the detector arrays. Each array incorporates a column of 90 indium antimonide photovoltic linear detector elements. These two arrays are independent of each other and are covered by filters which pass selected wavebands of IR radiation in the 3 to 5 micrometer range. Each element has the angular dimensions of 2 X .3 milliradians with the larger being its height. Designated as the lead and the lag, these two arrays are separated by about one-half degree in azimuth. [Ref. 1: p. 17]

Thus, as the IRSTD scans the horizon the resulting IR image has a resolution of approximately 10⁻⁴ radians (0.00573°) in the horizontal plane and 0.23° in the vertical plane. The video system's smaller field of view can be remotely controlled using the control units listed above. Thus, for the video data to be of any use in the development of the signal processing algorithms, the camera's orientation must first be known, and, in order to determine the pixel-to-pixel correlation between the IR image and the video image, the position of the video camera needs to be known with the same kind of accuracy as the IR image. The design and implementation of a position measuring system for this remotely controlled video camera is the subject of this thesis.

B. DESIGN SPECIFICATIONS

The design specifications for this problem were relatively straight forward. The position measuring system needed to meet the following criteria.

- The system should be able to measure the elevation angle (tilt), above and below the horizontal reference plane of the camera over a range of \pm 12°.
- The measured elevation angle should be accurate to within $\pm\,0.23^\circ$.

- The system should be able to measure the bearing (pan), left or right of some arbitrary reference, of the camera over a range of 360°.
- The measured bearing should be accurate to within $\pm 10^{-4}$ radians.
- The output should be displayed in a convenient form. The display should be collocated with the camera servo remote controls, an indoor site approximately 200 meters away from the camera.
- Portions of the measuring system required to be collocated with the camera should be weatherproofed.
- The system must be reliable and should be simple to operate.

II. DESIGN STRATEGY

A. GENERAL

A position measuring system, like any system, is a combination of devices interconnected to perform a certain function. The most basic position measuring system (see Figure 1) consists of only four such devices: a transducer, a signal conditioner, a display device and a power supply. More complicated position measuring systems include those designed to take a number of different measurements either simultaneously or consecutively. Still more complex systems multiplex these various measurements over a single channel to some distant location where they can be processed and displayed. [Ref. 2: pp. 2-14]

The design specifications for the camera position measurement system (subsequently referred to as the "measurement system") required that two measurements, pan and tilt, be taken simultaneously and transmitted some distance to a remote display. Two separate transducers, capable of independent operation, were therefore required. In order for both the azimuth and the elevation to be displayed simultaneously two display devices were also required.

Several pairs of RG-178 coaxial cable were available to transmit signals between the camera servo and the remote control site. Since the cable was available and it was desirable to reduce the system complexity, a decision was made not to multiplex the data over a single channel. Instead, each measurand would have a separate transducer, a dedicated signal processor and a unique display device. Position information for each axis would be transmitted over a dedicated channel.

The physical locations of the transducers and the display devices were dictated by the design specifications; however, there was some flexibility in deciding where to locate the signal conditioner. Site selection was based on an attempt to maximize total system performance and simplicity while ensuring the maintainability and environmental integrity of the signal conditioner. The only advantage to locating the signal conditioner with the camera servo and the transducer would have been to limit the distance that the transducer's output signal would have to be transmitted to the processor. On the other hand, separating the signal conditioner and the transducers would limit the distance over which the conditioned signal would have to be transmitted to the display device. The trade-off here was not clear cut and would probably depend on the specific hardware

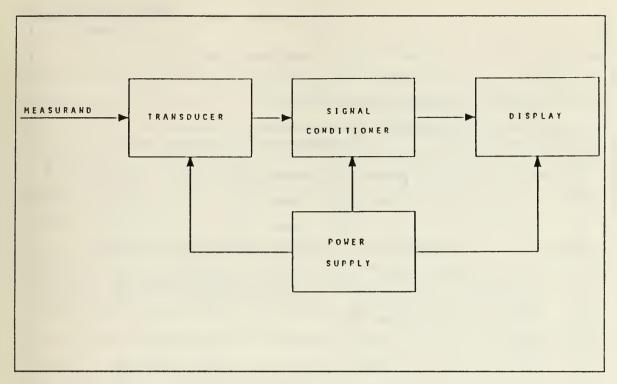


Figure 1. Basic Electronic Position Measuring System: From Ref. 2: p. 2

used and the speed of rotation of the camera servo. There was one significant advantage, however, to collocating the display and the signal processor; since they would both be indoors, the need for weatherproofing the signal processor would be eliminated.

Power was available at both ends of the system, there was therefore no requirement to have a common power supply for the entire system. One supply could be used to provide power to the two transducers, collocated with the camera servo, and a second supply could power the signal conditioner and the displays.

A block diagram of the prototype measurement system is shown interconnected with the camera positioning system in Figure 2. Once this basic system layout had been determined, proper selection of the actual hardware was necessary. The design criteria were the primary consideration in the initial stages of the hardware selection. Final selection of the specific components, however, involved balancing additional factors, such as availability and cost against the system requirements.

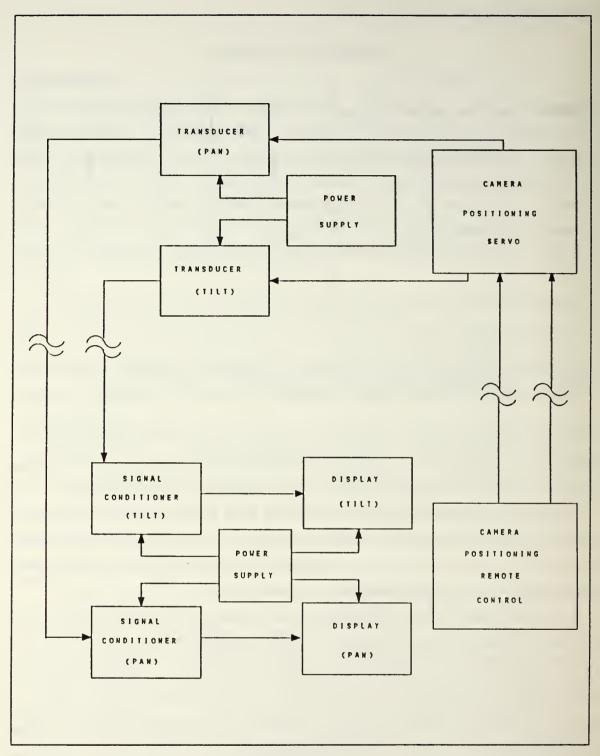


Figure 2. Camera Position Measuring System

B. TRANSDUCERS

1. General

Since in practice most measurement systems do not have the ability to respond directly to the measurand, transducers are used to convert one physical quantity (e.g., angular position) into another, more usable quantity or signal (e.g., an electrical signal) [Ref. 3: p. 1-4]. The transducer is therefore a vital part of any measurement system, and although none of the components of this system could have been chosen independently of the other elements, proper transducer selection appeared to be the key to meeting the design specifications. Thus, selection of a transducer was the next step in the design process.

Using the selection guidelines given by Norton on pages 51-53 of Ref. 2 and the design criteria stated previously, several observations and decisions were made which significantly reduced the number of transducers considered feasible for use in the measurement system. The fact that the servo was capable of rotating the camera left or right, and up or down suggested that the transducer should be capable of detecting both increasing and decreasing angles on both axes. Additionally, since the servo was anticipated to rotate the camera through one 360° arc in the horizontal plane, the transducer used to measure this angle (subsequently referred to as the "pan transducer") needed to have a comparable range capability. The range requirement for the "tilt transducer" (used to measure the elevation angle) was much less restrictive. These factors, angular bidirectional capability and full scale range, eliminated a great number of transducers from the list of candidates.

The list was further narrowed by the accuracy requirements previously specified. Again the accuracy in the horizontal plane placed a much more severe limitation on the selection of a transducer than the accuracy requirements for the vertical plane. The following paragraphs in this section outline the logic used in the selection of the transducers. The factors considered in the selection process included the following;

- The accuracy requirements given in the specifications.
- The ease with which a specific transducer could be installed on the servo.
- The ability to weatherproof the servo and the transducer once the transducer was installed.
- The rotation speed of the camera about the servo axes.
- The extent to which a particular transducer/mounting configuration would modify the measurand.
- Cost effectiveness.

- Availability.
- Signal conditioning requirements.
- The extent to which the selection of a particular transducer would simplify or complicate the modification or expansion of the measurement system.

2. Transducer technologies

Displacement transducer technologies fall into three very broad categories depending on whether they are capable of measuring linear or angular displacement, or both. Some technologies could be eliminated immediately since they were clearly not suited for measuring angular position. Strain gauge displacement transducers, inductive displacement transducers and vibrating-wire displacement transducers are examples of such devices. The following paragraphs briefly describe the different transducer technologies which were investigated. Table 1 on page 18 summarizes the salient points of the discussion. [Ref. 2: pp. 90-117].

a. Reluctive Displacement Transducers

The rotary variable differential transformer (RVDT), which operates by detecting a change in the reluctance between coils, offers excellent resolution, dynamic characteristics, linearity and life expectancy [Ref.3: p. (2-14)]. Figure 3 shows a schematic diagram and a simplified cross-section of an RVDT. The ferromagnetic, cardioid-shaped core is attached to a shaft as shown. As the shaft rotates, the inductive coupling between the primary and each of the secondary coils changes. When the cam is symmetric with respect to the two secondary coils, their output voltages are equal but opposite in phase which results in a differential output voltage of zero. As the shaft rotates away from this "null" the differential output voltage varies as shown in Figure 4. The linear region of the curve is limited to the angles between \pm 40° of the reference. Thus, the RVDT could not be used on the Pan axis. It was however, initially considered as a candidate for the Tilt transducer. [Refs. 2: pp. 93-99, 3: pp. (9-10)-(9-13) and 4: p. 19]

Another type of reluctive displacement transducer is manufactured by Farrand Controls. Their INDUCTOSYN rotary position transducers have accuracies to \pm 1.5 arc sec (\approx (4 × 10⁻⁴)°). Unfortunately, these devices are 11.89 inches in diameter, and mounting them on the camera servo would have been extremely difficult, if not impossible. [Refs. 2: pp. 89-111, 5]

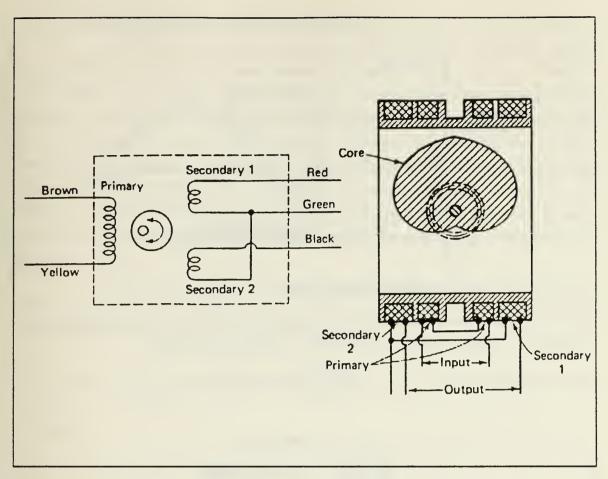


Figure 3. RVDT Schematic: From Ref. 2: p. 98.

b. Capacitive Displacement Transducers

Angular displacement can also be measured by coupling the rotating component to the shaft a of variable capacitor in the manner shown in Figure 5. Lenk describes the operation of the capacitive displacement transducer quite succinctly.

The capacitor ... consists of a metal plate that moves between two fixed metal plates as a shaft is rotated. The three plates, and the air between them, form a capacitor with a capacitance that varies in proportion to the degree to which the plates are meshed. When the plates are completely meshed, the capacitance is at its maximum. When the plates are completely unmeshed, the capacitance is at minimum. [Ref. 4: p. 18]

Capacitive displacement transducers offer many of the advantages of reluctance displacement transducers. They have an effective range of about 300° which, while better than the RVDT's range, is still not adequate for the pan axis [Ref. 4: p. 18]. Additionally they are more sensitive to changes in the ambient temperature. Since the

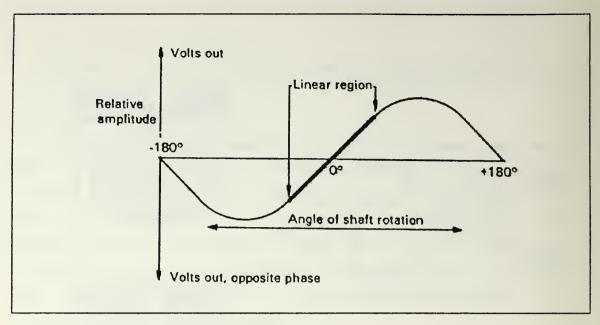


Figure 4. RVDT Output Characteristics: From Ref. 2: p. 95.

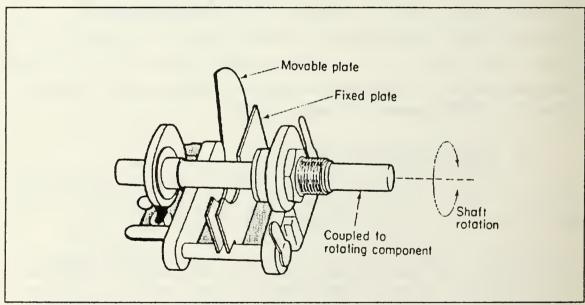


Figure 5. Capacitive Displacement Transducer: Ref. 4: p. 18.

measurement system was being designed to be used outdoors, the use of a capacitive displacement transducer would have required the addition of a temperature compensator in the design. While possible, this would have increased the system complexity considerably. [Ref. 2: pp. 90-91]

c. Potentiometric Displacement Transducers

Another very common and relatively simple family of transducers operate by measuring the change in resistance caused by a change in the measurand. There are a wide variety of such devices available. The basic form of potentiometric angular displacement transducers uses a resistance element, formed into an arc, and a movable electrical contact that rotates about the axis of interest. By measuring the change in resistance that results from a change in position, one is able to determine the angular displacement. The resistive element is typically a wirewound element, the resolution of which is determined by the number of turns per unit length of the resistance element. The angular resolution can be increased by increasing the turn density (wires/degree) of the potentiometer.

The practical limit for wire spacing on wirewound elements according to Ref. 6 is between 500 and 1000 turns per inch. From Figure 6 one can see that this limits the angular resolution for a single-turn device to

$$\Delta\theta(\text{rad}) \simeq \tan\left(\frac{\Delta x \text{ (in)}}{R(\text{in)}}\right)$$
 (1)

Therefore,

$$\Delta\theta(\text{rad}) \simeq \frac{2\Delta x}{D} = \frac{0.002(\text{in})}{D(\text{in})} . \tag{2}$$

To achieve the 10⁻⁴ rad resolution, specified for the Pan axis, with a single turn potentiometer would therefore require a 20 in diameter potentiometer. Mounting a device this large on the camera servo was simply not feasible. Potentiometers are, however, available with multiple turns. Shaped in a helix fashion similar to that shown in Figure 7, the total length of the potentiometer can be increased, which in turn increases its resolution, without increasing the diameter of the device.

Increasing the resolution of the potentiometer by increasing the turn density in any of the manners described above, however, increases the output impedance of the device, which leads to increasing nonlinearity between the measurand and the transducer

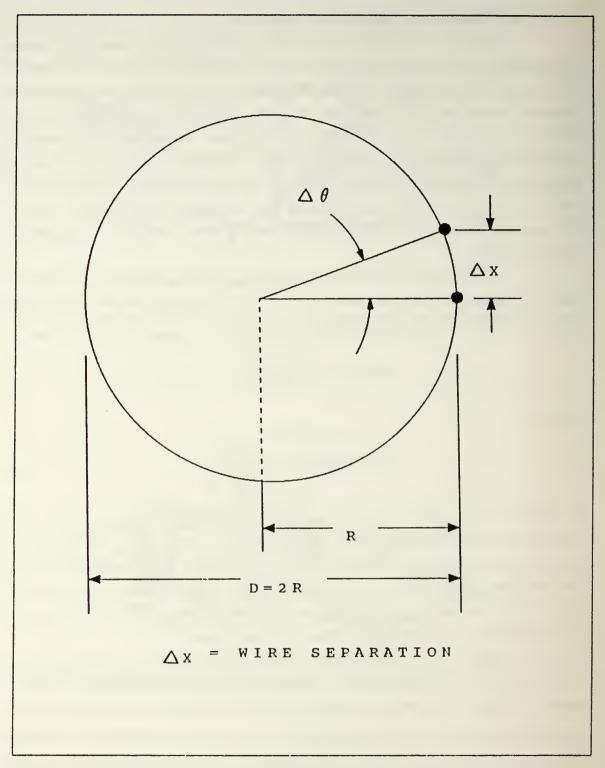


Figure 6. Geometry of an Angular Potentiometric Transducer

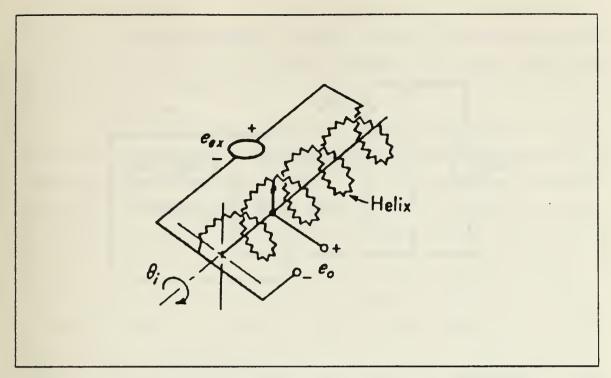


Figure 7. Multiturn Potentiometer: From Ref. 6: p. 218

output. The nonlinear relationship can be seen by analyzing the circuit shown in Figure 8. In the diagram the following variable definitions apply:

- $e_{\rm X}$ = Input voltage,
- $e_o =$ Output voltage,
- $R_p = \text{Total resistance of the potentiometer}$,
- $R_m = Meter resistance$,
- $x_r = \text{Total range of the potentiometer, and}$
- $x_i =$ Actual displacement of the potentiometer.

Assuming that R_p is uniformly distributed over x_n analysis of the voltage divider circuit gives,

$$\frac{e_o}{e_X} = \frac{1}{\frac{x_t}{x_i} + \left(\frac{R_p}{R_m}\right) \left(1 - \frac{x_i}{x_t}\right)} \quad . \tag{3}$$

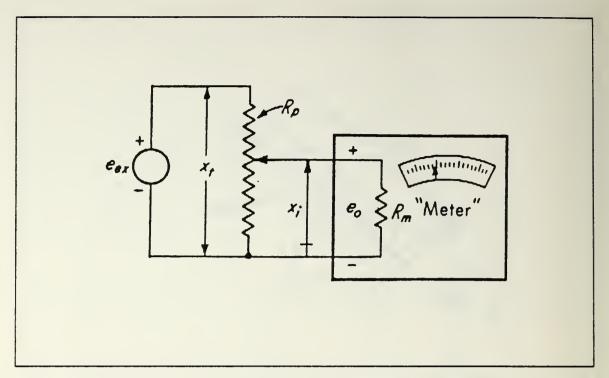


Figure 8. Potentiometric Transducer: From Ref. 6: p. 219

Thus, the ideal (i.e., linear) relationship,

$$\frac{e_o}{e_X} = \frac{x_i}{x_l} \quad , \tag{4}$$

is true only when R_p $R_m = 0$, and since $R_p \neq 0$, and $R_m \neq \infty$, the nonlinear relationship in (3) will always exist. Doebelin states that "for values of $R_p/R_m < 0.1$ the position of maximum error occurs in the neighborhood of $x_i/x_i = 0.67$, and the maximum error is approximately $15(R_p/R_m)$ percent of full scale." [Ref. 6: p. 218] Other potentiometric transducers, which use a resistive element made of carbon film or a conducting plastic, are not subject to the same kind of resolution limitations as wirewound devices; however, they do have high output impedances and the corresponding nonlinearities described above. [Ref. 6: pp. 217-224]

A high quality multiturn potentiometer used in conjunction with a high quality voltmeter offered one possible solution to the design problem. However, the nonlinearity of this arrangement was a significant disadvantage, and the primary reason why potentiometers were not used.

d. Encoders

The angular displacement transducer, referred to in general as an angular encoder or shaft encoder, converts an angular displacement into a digital signal without the use of an analog-to-digital converter. In today's increasingly digital world this can be a distinct advantage.

There are three different transduction methods used in encoders. Magnetic encoders use a pattern made from magnetized and nonmagnetized segments and one or more magnetic sensors that register as either "1's" or "0's" depending on the magnetic characteristics of the section that they are adjacent to. Brush-type encoders are similar, but the sections are made of conducting and nonconducting materials. The conductors are all tied to a common source and the "sensor" is one or more brushes connected to the output. When the brush is in contact with one of the conductors the output is "on" and when the brush is in contact with an insulator the output is "off". Optical encoders (See Figure 9) use a pattern of opaque sections marked on an otherwise transparent disk. A light emitting diode (LED), or other light source, is placed on one side of the disk, and as the disk rotates a light sensor on the other side of the disk "sees" periods of dark and light which it converts into a digital signal. [Ref. 2: p. 106]

Angular encoders are further categorized as either absolute encoders or incremental encoders. Absolute encoders, similar to the optical encoder shown in Figure 9, use a multitrack pattern on a code wheel to produce a unique coded output signal for each incremental change in the measurand. These wheels use a variety of codes, including binary code, binary-coded decimal (BCD) and Gray code, to determine the shaft position. The resolution of an absolute shaft encoder is limited by the number of tracks on the disk and the type of code used. A simple binary or Gray code encoder, which are more efficient than the BCD encoders, with N tracks has an optimum angular resolution of

$$\Delta\theta = \frac{360^{\circ}}{2^{N}} \quad . \tag{5}$$

Thus, to achieve the desired resolution of 10^{-4} radians on the Pan axis with an absolute encoder would require a code wheel with $N \ge 16$. Since the output from the encoder is unique for each position, these devices are not affected by power outages, and the requirements for a signal processor for such a device would be limited to a simple decoding circuit. These encoders can measure angles of up to 360° without ambiguity.

Incremental encoders use a code wheel which has only one track. As the shaft of the incremental encoder rotates the output from the encoder is a series of equally spaced pulses. These pulses can then be used as an input signal to an up/down (U/D) counter of some sort. The output from the counter is an indication of the displacement of the axis from some predetermined reference. The resolution of an incremental encoder is a function of the number of pulses the code wheel generates per revolution and is given by;

$$\Delta\theta = \frac{360^{\circ}}{\text{n} \times \text{PPR}} \tag{6}$$

where PPR is the number of pulses per revolution of the code wheel, and n is the number of revolutions that the code wheel makes per revolution of the axis of interest. If the incremental shaft encoder was mounted on the shaft of interest (n = 1) at least 62,832 PPR would be required to ensure a resolution of 10^{-4} radians.

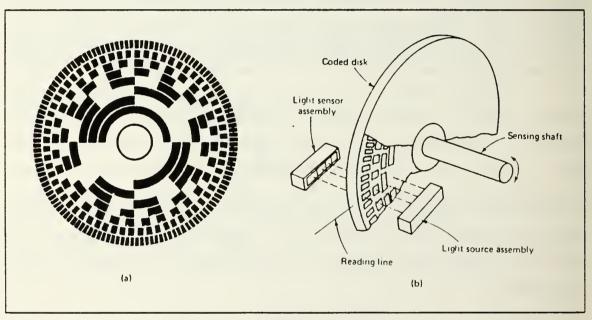


Figure 9. Absolute Photoelectric Angular Encoder: (a) typical code disk; (b) encoder elements. From Ref. 2: p. 107.

Shaft encoders currently range in price from less than \$100.00 to several thousand dollars depending on their capabilities and the method of transduction used. Litton Encoder's Model 60 absolute shaft encoder uses a natural binary code, has 15 tracks (0.1917 mrad resolution) and is available "off the shelf" for approximately \$3000.

Other absolute encoders with comparable resolutions are available at similar prices. No incremental encoders were found which offered the same kind of resolution as Litton's Model 60; however, because they are not limited to one revolution of the axis, the resolution of an incremental encoder can be improved by a factor of n by causing its code wheel to rotate n times for every rotation of the axis of interest. Incremental encoders with 1024 PPR are available from a variety of manufacturers for about \$100 each. Connecting such a device to the axis of interest via a gear train with a 50:1 ratio would theoretically result (from (6)) in a resolution of 0.1227 mrad. Incremental encoders do require more complex signal processing than absolute encoders, and they are affected by power shut-off. Additionally, unlike absolute encoders, any missed or erroneous count that occurs with an incremental encoder will cause a persistent error. [Ref. 7: p. 16]

After considering the measurement system performance criteria and the capabilities and limitations of the various transducers, the use of an incremental, optical shaft encoder appeared to be the best selection for the transducer for each axis. This decision involved balancing the various advantages and disadvantages of the different transducers. The following list gives a summary of the key considerations in this decision.

- Small, lightweight, highly accurate and relatively inexpensive models were readily available. Being small and lightweight suggested that mounting and weatherproofing the transducers in the camera servo should not be too difficult.
- Absolute encoders offer almost all of the advantages of the incremental encoders; they are not affected by power outage, they require less complex signal processing and one time counting errors do not persist. However, these features did not seem to justify the additional price of an absolute encoder.
- Linearity and loading problems associated with the potentiometric displacement transducers were avoided.
- Direct conversion of the measurand into a digital signal precluded the requirement for an A'D converter. (This would have been a disadvantage had the use of an analog signal conditioner been anticipated.)
- Using two identical transducers, each capable of meeting the specifications for the pan axis, would reduce system complexity while still ensuring that the design specifications were met.

C. MOUNTING THE TRANSDUCER

Once the decision to use an incremental optical shaft encoder was made, selection of a specific model remained. Before selection of an actual piece of hardware could be

Table 1. ANGULAR DISPLACEMENT TRANSDUCERS

TRANSDUCER DESIGN	RANGE	RESOL- UTION	LINEAR- ITY	OTHER
Reluctive Displacement (RVDT)	0° -360°	Theore- tically infi- nite: Limited by the signal condi- tioner.	Poor beyond ± 40°	
Reluctive Displacement (Farrand's INDUCTOSYN)	0° -360°	± (4 × 10 ⁻⁴)°	Good	Large size limits use- fulness with the cam- era measuring system.
Capacitive Displacement	0° -300°	Theore- tically infi- nite: Limited by the signal condi- tioner.	Good	Temperature sensitive
Potentiometric Displacement	0° -3500°	Device dependent	Device dependent	The trade-off be- tween range resolution and linearity due to the loading effect of the noninfinite impedance of the sig- nal conditioning de- vices used.
Absolute Encoders	0° -360°	360° 2°	Good	No A D conversion required. Insensitive to power shut-off.
Incremental Encoders	±∞	$\frac{360^{\circ}}{\text{n} \times \text{PPR}}$	Good	Simple. Requires more signal processing than absolute encoder but is less expensive.

done though, one additional practical consideration had to be made; where and how could a transducer be mounted in or on the servo in order to measure the position of the Pan and Tilt axes?

The physical layout of the camera positioning servo made direct connection of any type of transducer to the axes of interest virtually impossible without major modification of the servo itself. Major modification of the servo would have been expensive, time consuming and outside the scope of this thesis. It was not considered an option in this case. Measurement of the Pan and Tilt axes' displacements was most readily accomplished indirectly. Each axis of the servo is positioned by a separate dc motor via a gear train. By mounting the shaft encoder code wheels to the sprockets (items 42 and 43 in

Figure 10) which are each attached to one of the worms, an indirect measurement of the position of each of the wormgears (items 5 and 7 in Figure 10) was possible. This approach, made necessary by the servo design, was a mixed blessing.

The backlash in a worm-wormgear connection will cause the position of the worm to be different for any given wormgear position, depending on whether that position is approached from a clockwise or a counterclockwise direction. In order to correctly determine the displacement of the wormgear by measuring the displacement of the worm, the amount of backlash present must be known (i.e., would have to be determined experimentally) and accounted for by the measurement system. This nonlinear source of error would not have been a concern if the servo was only required to rotate in one direction. This was not the case, however, and hysteresis eventually was determined to be the largest single source of error in the measurement system. A more complete discussion of this topic is included in Chapter IV of this thesis.

Assuming for the moment that the effects of the backlash in the gears could have been completely compensated for, mounting the shaft encoders on the worm provided a measurement advantage analogous to the mechanical advantage afforded by the gear train. Initial measurements indicated that each of the worms turned through $18,000^{\circ}$ ($50 \times 360^{\circ}$) for every 360° rotation of the corresponding wormgear. This meant that a shaft encoder with 100 divisions per 360° attached to the worm axis could do the same job as a 5,000 division per 360° encoder attached to the wormgear axis.

D. SELECTING AN OPTICAL SHAFT ENCODER

Once the basic decisions to use incremental optical shaft encoders and to mount the encoders on the worms inside the servo housing had been made, selection of the specific pieces of hardware was relatively straight forward and was primarily a matter of convenience and expediency.

Returning to the design specifications for a moment; the most stringent requirement was to be able to measure the position of the pan axis to within $\pm (5.73 \times 10^{-3})^{\circ}$. To determine the required resolution for the optical shaft encoder, the following calculations were performed.

First,

$$\frac{360^{\circ}/\text{Revolution}}{5.73 \times 10^{-3}^{\circ}/\text{Division}} \simeq 62,827 \frac{\text{Divisions}}{\text{Revolution}} . \tag{7}$$

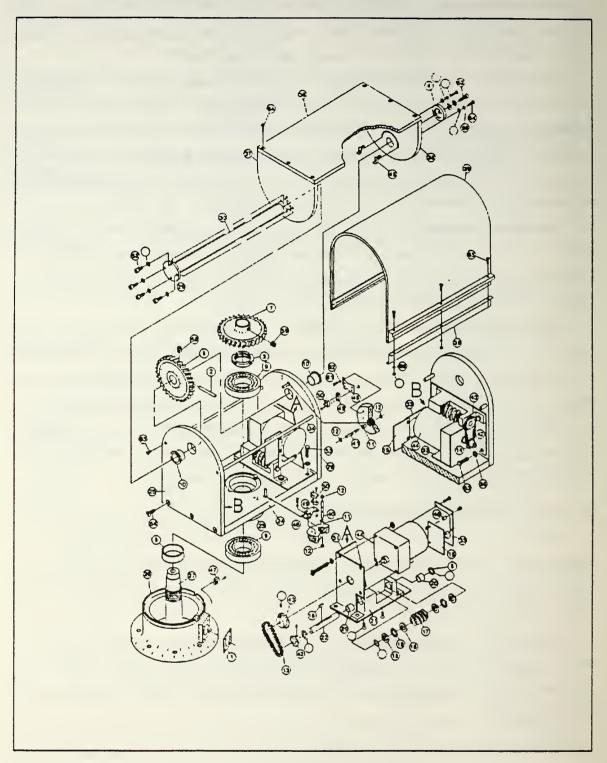


Figure 10. Camera Servo: From Ref. 8: p. 12.

Then, considering the 50:1 gear advantage,

$$\frac{62.827}{50} \approx 1257 \frac{\text{Divisions}}{\text{Revolution}} \ . \tag{8}$$

The task therefore was to find an optical shaft encoder capable of detecting bidirectional rotation with at least 1257 Divisions/Revolution in a package small enough to mount in the servo housing on the worm axis. There was no absolute size limitation; however, due to the construction of the servo it was desirable to find an encoder that was no more than 3 in. in diameter and no more than 1.5 in. in width. The companies that make shaft encoders are capable of custom building devices to meet a customer's specific needs. However, the prices are high, and the lead times are long for these special order parts. The encoder for this system needed to be reasonably priced and readily available to ensure timely completion of the project and to facilitate replacement, if necessary, in the future.

Optical shaft encoders are manufactured by numerous companies including Litton, Honeywell, BEI, IVO and Hewlett Packard. Sales literature from these companies was reviewed prior to making a decision on the specific shaft encoder model to be used. Incremental optical shaft encoders with resolutions that range from one pulse per revolution (PPR) to 2540 PPR are available off the shelf from one or more of these companies. While evaluating sources of supply, incremental optical shaft encoders were also found in use in various laboratories and shops in the Electrical Engineering and Physics Departments at the NPS. Encoders immediately available from stock included two Vernitech 1200 PPR (model VOE-23-1200-AI-LD5-2L1-1603-2) encoders from the Physics Department and two Hewlett Packard (HEDS-6000, J06) encoders from the Electrical Engineering Department. The use of the Vernitech encoders was ruled out because they were unable to detect bidirectional movement without increasing the complexity of the signal conditioning subsystem. Additionally, technical literature requested on two separate occasions from Vernitech was never received.

The HEDS-6000/J06 encoders have a resolution of 1024 PPR. Each encoder provides displacement information in the form of TTL logic level signals via two output channels. When the encoder is properly adjusted the two output signals have a 90° phase difference. This quadrature phase relationship permits these encoders to detect bidirectional displacements. Rotation in one direction will cause Channel A to lead

Channel B (in phase), while rotation in the other direction will cause Channel B to lead Channel A. [Ref. 9: p. 2]

The presence of two output channels in quadrature phase has an additional benefit that is useful in some applications. Since the amount of position information has essentially been doubled, if the signal conditioner is designed to detect both the leading and trailing edges of one of the output channels the resolution of the measurement system can be doubled. The difficulty with using this technique is that multiple oscillations about a single point cannot be detected as such. If the camera were to oscillate less than one half of a pulse width about a transition the signal conditioner would detect and erroneously count the multiple transitions. [Ref. 7: pp. 13-16]

With 1024 PPR, which is less than the 1257 PPR required to meet the 0.1 milliradian accuracy specification on the pan axis, the maximum resolution available, if the HEDS-6000 was attached to the worm, can be calculated as;

$$\frac{360^{\circ}}{(50 \times 1024)} = (7.03125 \times 10^{-3})^{\circ} \text{ Pulse}^{-1} . \tag{9}$$

Although this was not sufficient to satisfy the pan axis resolution specification of $(5.73 \times 10^{-3})^{\circ}$ Pulse,⁻¹ all of the other performance criteria could be satisfied. The trade-off seemed reasonable and was approved prior to proceeding further with the system design.

E. THE DISPLAY

Selecting a method to display the final system output was certainly the least demanding task required in the design of the system. With an expected resolution on the pan axis of approximately 0.007° over a range of 360° (a ratio of about 1:51,500) an analog display seemed out of the question. A five or six digit digital display on the other hand offered a simple, reliable and cost efficient means of presenting the output. Constructing the displays from individual, seven-segment, common anode, LED devices, and the appropriate display drivers was a straight forward task.

F. THE SIGNAL CONDITIONER

Anticipating the use of two incremental shaft encoders as the transducers for the measurement system and the use of digital readouts as the display devices significantly reduced the number of possibilities for the signal conditioning subsystem. In addition to the hardware and software described in each of the subsequent discussions, each

technique listed here would require an edge detector to detect the transitions in the TTL signals from the shaft encoders.

- Up/down counter with table look-up.
- Up/down counter and multiplication.
- Add/subtract.
- Microcomputer.
- Microprocessor.

1. Up/down (U/D) counter with table look-up

This technique would involve the use of a shift register, some associated logic, an U/D counter and a table look-up device such as an erasable programmable read only memory (EPROM). The shift register would serve as a hardware buffer that could be used to account for the hysteresis introduced by the worm-wormgear assembly. The length of the buffer would have to be determined experimentally. The logic associated with the shift register would determine the "validity" of each transition (count) signal from the edge detector by checking the contents of the shift register and comparing the current direction of rotation with the previous direction of rotation. Whenever the logic detected a change in rotation direction, or a partially full, or a partially empty buffer (depending on the direction of rotation), the transition would not represent a "valid" count since any of these conditions would indicate that the transition was due to a change in the position of the worm without a corresponding change in the position of the wormgear. Thus, the present transition would be the result of hysteresis due to the backlash in the gear train and the transition would be "invalid". Such a transition would cause the contents of the hysteresis buffer to be modified appropriately. A more complete discussion of this topic is contained in Chapter IV. The shift register and associated logic could be built from common TTL devices readily available at the NPS.

Once a count had been determined to be valid, an U/D counter would be used to keep a running total of the number of counts. Again, such a device could be built using readily available TTL devices such as the 74LS168A, Synchronous 4-Bit Up/Down Decade Counter, or the 74LS169A, Synchronous 4-Bit Up/Down Binary Counter. The output from the U/D counter would then be used as an address to "look up" a predetermined number stored in an EPROM.

This design approach was considered relatively straightforward, and at least initially seemed like a viable option. Its major advantage was that it was conceptually quite simple. This simplicity had a price though; it would have been very hardware in-

tensive and consequently would have been a very inflexible design. For example, if at a later date the use of an arbitrary reference was desired, additional hardware would have to be added to the signal conditioner so that the counter could be initialized to the arbitrary starting point. Since all of the processing would have to be done in hardware, even a minor modification in the system could necessitate a major design revision. Another consideration was that saving in excess of 51,000 unique positions in the EPROM presented a nontrivial problem that would need to be solved if this technique was used.

2. Up/down counter and multiplication

This is very similar to the previous case, differing only in that instead of looking up a predetermined position, in a memory device, a multiplier would be used to multiply the output of the U/D counter by a predetermined constant. As an example, if experimental results indicated that the shaft encoders generated one pulse for every 0.00703125° that the camera was displaced, then each time a valid count was received, the updated count would need to be multiplied by 0.00703125 in the final stage of the signal processor. The result would be the new position. Again, while conceptually simple this idea had some significant disadvantages. Even more hardware intensive than the first approach, this design would also have extremely limited flexibility.

Accomplishing the multiplication would have posed a formidable task. The scale factor would have to be written as some integer (e.g., 0.00703125 would become 703125, or 70323, or 7031, etc.) depending on the desired accuracy. The count, already an integer, would be multiplied by the constant and the correct position of the decimal point would have to be determined. Locating the decimal point would be a relatively simple task, but multiplication of two numbers such as 51,000 and 70,313 would not be as easy. At least one 16 bit by 16 bit binary multiplier (i.e., TRW's MPY016H) is currently available, but since the number 70313 cannot be represented in binary by less than 17 bits, the multiplication could have been accomplished in either of two ways. One solution would have been to perform the multiplication in two or more stages. Alternatively, 70313 could be "rounded" to 7031. The second option would create a cumulative round-off of about $(1.28 \times 10^{-3})^{\circ}$ per 360° rotation (assuming 51,200 pulses per 360°). This round-off error would probably have been acceptable, but the complexity and limited flexibility of either multiplication scheme made the U/D counter and multiplication an unacceptable candidate for the signal processing subsystem.

3. Add/subtract

A third design concept considered the elimination of the U/D counter altogether. The same logic proposed for use in the previous two designs could have been

used to check the validity of a count and to determine the direction of rotation. However, instead of valid counts being sent to an U/D counter as before, these counts would now signal an adder to add or subtract a predetermined constant from the running total. Just as before, this simple idea could probably have been made to work at least once, but its usefulness as a part of a larger system would certainly have been limited. The large number of components required to realize this design would have increased the probability of failure, complicated troubleshooting and reduced overall flexibility.

4. Microcomputer

If the signal processing subsystem was built around a microcomputer (PC), virtually all of the disadvantages associated with the previously discussed approaches would be eliminated. Since all of the logic could be implemented in software, modifications to the system would be relatively simple to make, and the system's flexibility would be enhanced. However, dedicating a microcomputer, even an inexpensive model, to the signal processing tasks for this measurement system was considered overkill, and timesharing with one of the PC's already in service was possible, but not considered practical or convenient since these microcomputers had already been dedicated to a variety of tasks.

5. Microprocessor

One final option for the signal processor remained. Microprocessors are relatively inexpensive and powerful and are available in a wide variety of makes and models. If a microprocessor was used instead of a microcomputer or a straight hardware processor, the "nice to have" requirements such as flexibility, ease of modification and capacity for expansion, as well as the required signal processing functions could all be satisfied. On the other hand, microprocessors have one distinct disadvantage; they are not user friendly. The use of a microprocessor implied countless hours spent tracking individual bits, debugging assembly language code, studying timing diagrams, etc.. No matter how distasteful the thought, however, a microprocessor was clearly the best way to perform the signal processing functions of the measurement system.

As with the selection of the transducer, once the basic design approach had been determined, selection of a specific device was a relatively straight forward task. The choice of one microprocessor over another was a function of the processor's ability to perform the required tasks, cost effectiveness and availability. Motorola's MC68705U3 seemed to satisfy all of these requirements. The MC68705U3 is a four kilobyte EPROM microprocessor, built using HMOS (high-density NMOS) technology with an eight bit architecture. The "68705" operates on a 5.0 volt dc supply, has 112 bytes of on chip RAM, four vectored interrupts, 24 TTL/CMOS compatible bidirectional I/O lines (eight

lines are LED compatible), eight dedicated input lines and an internal eight bit timer with a seven bit programmable prescaler. [Ref. 10: p. 1]

In Ref. 10 Motorola advertises the following software features:

- Programming language similar to the 6800 family.
- Byte efficient instruction set.
- Easy to program.
- True bit manipulation.
- Bit test and branch instructions.
- Versatile interrupt handling.
- Powerful indexed addressing for tables.
- Versatile index register.
- A full set of conditional branches.
- Memory usable as registers/flags.
- Single instruction memory examine/change capability.
- Ten powerful addressing modes.
- All addressing modes apply to EPROM, RAM and I/O.

One key advantage to using the MC68705U3 was that one of the microprocessors, and a Motorola M68705EVM (the evaluation/programming module for the M6805 family of devices) were both available for immediate use at the NPS. The fact that the 68705 utilized HMOS technology suggested that it should be a relatively low cost microprocessor. In fact, except for the price of a phone call, a second microprocessor was obtained free of charge from a local electronics wholesaler. Additional microprocessors, to be used as replacements and as backup devices were ordered for about \$20,00 each.

One potential problem with using a microprocessor begged checking prior to proceeding. Initial measurements of the camera's maximum rotation velocity produced the following results.

$$\omega_{PAN(\max)} \simeq 1.0 \text{ rpm}$$
 (10)

$$\omega_{TILT\,(\text{max})} \simeq 0.5 \text{ rpm}$$
 (11)

Again the requirements for the pan axis presented the most stringent design limitations. Since the optical shaft encoders were anticipated to deliver 51,200 PPR (1024×50) the

microprocessor on the pan axis had to be capable of processing 51,200 pulses/minute (1.172 ms / pulse). The MC68705U3 is designed to operate with an oscillator frequency (f_{osc}) of between 0.4 MHz and 4.4 MHz and has an instruction cycle time $(4/f_{osc})$ of between 0.950 μ s and 10 μ s. Assuming that a 4.0 MHz clock was used, the instruction cycle time would be 1.0 μ s. This would mean that the processing of each pulse would have to be accomplished in no more than 1172 instruction cycles to ensure that no pulses would be missed.

III. DESIGN

A. GENERAL

The schematic diagrams for the measurement system are shown in Appendix A; Appendix B contains copies of the printed circuit board plans. Before describing the detailed operation of each of the individual components of the measurement system, a brief overview of its basic theory of operation is in order. The measurement system is actually two separate systems operating independently. The system designed to measure the azimuth or pan angle will subsequently be referred to as the "Pan System", and the other system, designed to measure the elevation or tilt angle, will be referred to as the "Tilt System". However, because the two systems are quite similar the discussion which follows will only specifically describe the operation of both systems where their operation differs.

In the most general terms, the measurement system shown in Figure 2 on page 6 uses two microprocessors to count the pulses generated by the incremental shaft encoders, and to provide output signals to the display devices. The counting function performed by each microprocessor involves determining the direction of rotation and determining whether each count is "valid". Valid counts are encoder pulses which result from the displacement of the camera servo, while invalid counts are a result of the hysteresis in the gear train. The number of valid counts is directly proportional to the angular displacement of the camera axis.

Both of the displays are capable of presenting the position information in two basic forms. In the Count Mode they display the number of pulses that have been detected, and in the Position Mode they display the angle in degrees that the number of pulses represents. A third display mode, which is a combination of the first two, is also available. In the third mode, referred to as the "Blinking Mode", the display will alternately display the count and the angle.

B. SHAFT ENCODER AND LINE DRIVER

Figure 11 shows the basic components of the HEDS-6000 incremental optical shaft encoder. The encoder is approximately 56 mm in diameter and 20 mm deep. The code wheel assemblies for the HEDS-6000 J06 encoders are designed to mount on 0.25 in. shafts. Since the mounting surface shown in Figure 11 is not part of the encoder kit, and did not existed on either of the worm axes, two such surfaces were machined in the

Physics Department Shop and attached to one end of each of the worms. Each surface has a 0.25 in diameter shaft to which one of the code wheel assemblies is attached. Two sheet metal brackets, also made in the Physics Department Shop, are bolted to the servo frame. The encoder bodies are mounted to these brackets. Figure 12 shows the shaft encoders mounted in the camera servo. [Ref. 9: p.1]

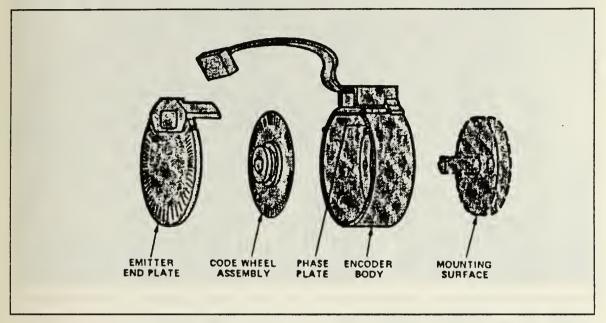


Figure 11. HEDS-6000 Series Encoder Kit: From Ref 9: p.6.

Also seen in Figure 12 is a printed circuit board mounted between the two optical shaft encoders. Each of the encoders is electrically connected to the board via a separate ten wire ribbon cable. The power and the output signals from the shaft encoders are transmitted through these cables. A sketch of the ribbon cable connector and the pinout for the connector are shown in Figure 13. Each connector is attached to a ten pin header on the printed circuit board. Pins 2, 7 and 9 are connected to a +5.0 Vdc power supply external to the camera servo. A description of the power supply is given later in this chapter. Pins 3, 4, 5 and 6 are connected to the power supply ground. The HEDS-6000 does not have an index pulse, therefore pin 10 is not connected.

The remaining two pins on each header connect the output channels of the shaft encoders to two 74S140 line drivers. Each 74S140 is a dual four-input NAND gate 50-Ohm line driver. The line drivers are powered by the same supply as the encoders. They serve as buffers between the encoders and the transmission lines which are used to transmit the encoder signals to the signal conditioner. The line drivers' typical high

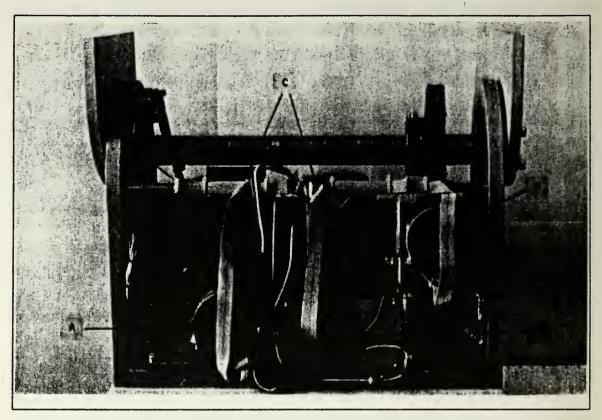


Figure 12. Modified Camera Servo: (a) Optical shaft encoder used to measure Pan axis displacement, (b) Optical shaft encoder used to measure Tilt axis displacement, (c) Ribbon cable, (d) Printed circuit board.

output current is 10 mA and the maximum is 18 mA. Resistance in the transmission line was measured to be approximately 35 Ω , and to be on the safe side a 10 Ω connector loss was assumed. The voltage drop due to an 18 mA current through a 45 Ω resistance is 0.81 V. A "voltage high" signal received at the signal conditioner should therefore be about 4.19 V. This is well above the maximum, positive-going threshold voltage specification of 2.0 V for the 7414 Schmitt triggers, which are used to receive the signals at the signal processor. [Ref. 11: pp. 5-73, 5-74, 6-44]

C. ENCODER-MICROPROCESSOR INTERFACE

The signals transmitted by the two line drivers are Channels A and B of each of the shaft encoders. These signals contain the raw data which the signal processor converts into position information. Three pairs of multiple pin connectors are used in the encoder-microprocessor interface. The pinouts for these connectors are shown in

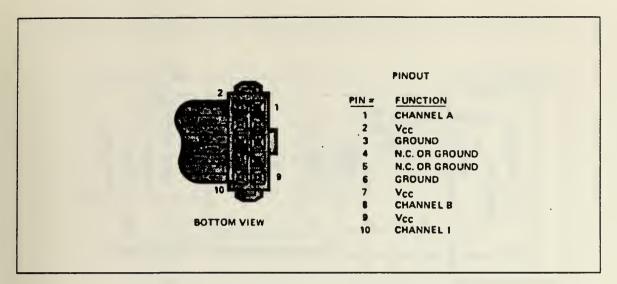


Figure 13. Encoder Connector Specifications: From Ref. 9: p. 6.

Figure 14. Each of the four signals is received at the signal processor by a 7414 Schmitt trigger which is used to "clean up" the signal. The Schmitt triggers lower the system's susceptibility to errors caused by slow state transitions and increase the signals' fan out capabilities [Ref. 7: p. 13].

The output of each Schmitt trigger is routed to an input port of the appropriate microprocessor. Each Channel A signal is also the input to an edge detector. The edge detectors each consist of three 7414 inverters, a 74LS86 EXOR gate and a 47 nF capacitor, configured in the manner shown in Figure 15. This configuration causes the interrupt line to go low for approximately 2 μ s each time Channel A transitions from low to high or from high to low. Since an oscillator frequency, f_{osc} , of 4.0 MHz is being used, the interrupt pulse width, t_{WL} , must be greater than or equal to 1.25 μ s [Ref. 10: p. 3]. The value of the capacitor required to achieve the 2 μ s delay was determined experimentally.

D. SWITCHES

The measurement system has 10 switches that allow the operator to control specific functions of the signal processors and the displays. Figure 16 shows the physical location of these switches on the control panel. Switches SW1(P) and SW1(T) control the reset lines to the microprocessors. Switches SW2(P), SW2(T) and SW5 control the display mode. The Function and Set switches; (SW3(P), SW3(T), SW4(P) and SW4(T)) allow the user to change the length of the hysteresis buffer in the microprocessor. The

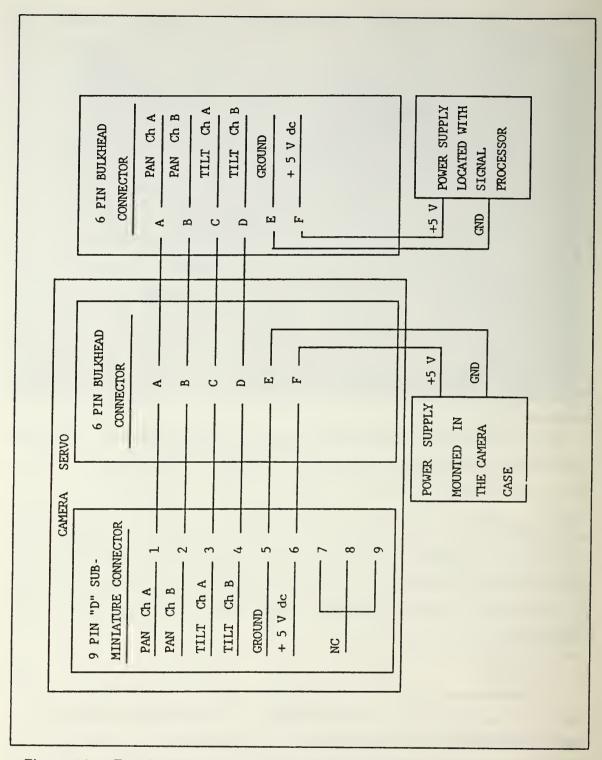


Figure 14. Encoder-Microprocessor Connector Specifications

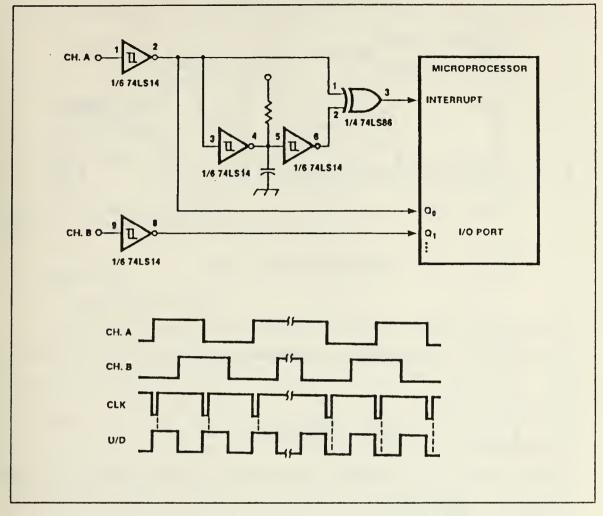


Figure 15. Interrupt Interface: After Ref 7: p. 14.

master power switch is SW6. Table 2 identifies the switches by name, description and function.

Any mechanical switch will "bounce" or "chatter" when it is thrown, and since the operation of the signal processor depends on the number of times that the Display Mode and Set switches change position, these switches had to be "debounced". A very simple but effective way to do this is with an \overline{RS} latch. Switches SW2(P), SW2(T), SW4(P) and SW4(T) are each debounced in this manner. Each latch is made from two 74S00 NAND gates connected in the manner shown in Figure 17. [Refs. 13: pp. 132-135, 12: pp. 3,4]

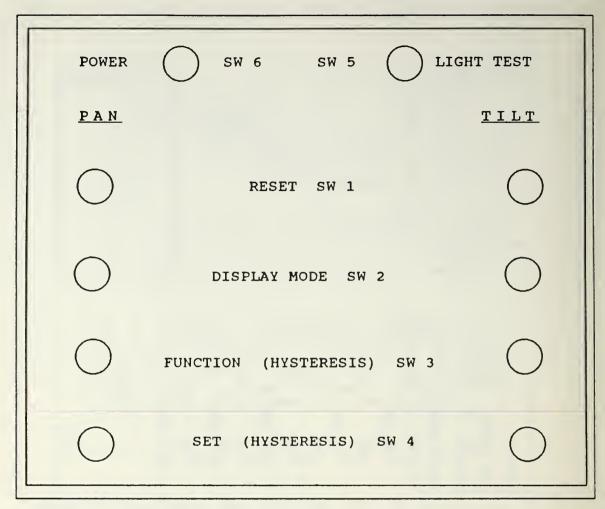


Figure 16. Control Panel

E. MC68705U3

1. General

The two 40 pin MC68705U3 microprocessors (MPU's) are the heart of the measurement system. With the exception of the light test signal, every signal in the system is either part of the input to one of the MPU's or part of their output. The MPU's were programmed using the assembly language syntax, assembler directives and instruction set for the M6805 family of microprocessors which are described in Ref. 14. The Pan and Tilt programs are listed and their operation is described in Appendix D. The pin assignments for the MC68705U3 are shown in Figure 18. Table 3 briefly describes the purpose of each pin and the actual connections for the two MPU's.

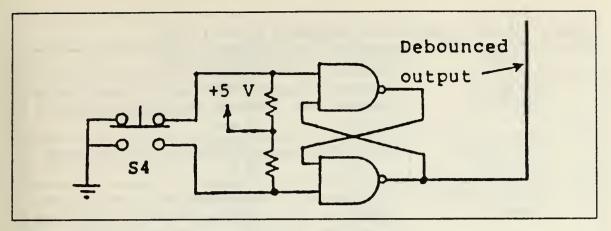


Figure 17. Debouncing circuit: After Ref 12: p. 4.

2. Memory Map

a. Input/Output (I/O)

The memory map for the MC68705U3 is shown in Figure 19. The digits following a "S" are the hexadecimal representation of the address for a specific memory location. The data registers occupy the first four memory locations of each MPU. Thus the information written into the registers at \$000, \$001 and \$002 is written to the output ports A, B and C respectively. Port D, at address \$003, is an input only port as indicated in Table 3. In order to determine the state of the input lines, the contents of the register at \$003 must be read by the MPU. Registers \$004, \$005 and \$006 are the data direction registers (DDR's) for Ports A, B and C respectively. Because all three ports are used as "output only" ports, in this application, the DDR's are all established as such by an initialization routine performed by the MPU's during their initial power-up and after each external reset. [Ref. 10: pp. 5, 12, 14]

Pin 18 of the MPU can be used as either a general purpose input line or as an interrupt line. The primary interrupt line on each MPU is used to signal the occurrence of a state transition on Channel A. Pin 18 is used as a second interrupt line to signal a display mode change request from the operator. The Miscellaneous Register (MR) at address S0A is used to control the operation of the second interrupt line (INT2). In order to establish pin 18 as an interrupt line, bit 6 of the MR is cleared by the Initialization Routine. The INT2 Interrupt Request Bit, bit 7 of the MR, is cleared by default upon reset. It is set when a falling edge is detected on the Display Mode line which is connected to pin 18. When this occurs and bit 6 of the MR is cleared, an interrupt request is generated. This interrupt request causes the display mode to change.

Table 2. SIGNAL PROCESSOR AND DISPLAY SWITCHES

NAME	DESCRIPTION AND FUNCTION				
PAN RESET (SW1(P))	Momentary action push button switch: Resets the Pan Microprocessor. Causes the Pan Display to be reset to zero.				
TILT RESET (SW1(T))	Same as SW1(P) except it affects the Tilt System only.				
PAN DISPLAY MODE (SW2(P))	Single pole double throw toggle switch: Each time the switch position is changed the Pan Display toggles from Count mode, to Position Mode, to Blinking Mode, to Count Mode, etc				
TILT DISPLAY MODE (SW2(T))	Same as SW2(P) except it affects the Tilt Display only.				
FUNCTION (HYSTERESIS) (SW3(P))	Single pole double throw switch: When closed, causes the "Function" line of the Pan Microprocessor to go low and causes the size of the hysteresis buffer to be displayed on the Pan Display. Enables SW4(P).				
FUNCTION (HYSTERESIS) (SW3(T))	Same as SW3(P) except it affects the Tilt System only.				
SET HYSTERESIS (SW4(P))	Single pole double throw switch: Inoperable unless SW3(P) is closed. If SW3(P) is closed, each time the position of SW4(P) is changed the length of the hysteresis buffer is incremented by one. Maximum buffer length is 25. Toggling SW4(P) when the buffer length is 25 will cause the buffer length to be reset to zero.				
SET HYSTERESIS (SW4(T))	Same as SW4(P) except it affects the Tilt Hysteresis buffer.				
LIGHT TEST (SW5)	Single pole single throw switch: When closed, lines 1, 2, 7, 8, 10, 11 and 13 on each of the LED displays will go low. Unless an element is burned out, every digit in both displays should be an eight.				
POWER (SW6)	Single pole single throw switch: When closed, applies + 5.0 V dc power to the signal processors and the displays.				

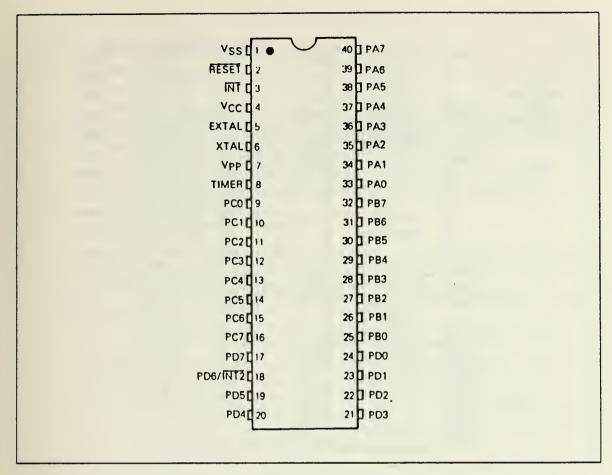


Figure 18. MC68705U3 Pin assignments: From Ref. 10: p. 1.

Once bit 7 has been set by an interrupt, it must be cleared by software to avoid repeated and unwanted interrupts from occurring. This task is performed by the Mode Change Routine in each EPROM. [Ref. 10: pp. 1, 10, 13, 15]

b. Timer

The operator can cause either or both of the displays to "blink" by using the Display Mode Switches, SW2(P) and SW2(T). When one of the systems has its display in the Blinking Mode, the associated MPU uses its timer to generate a timer interrupt request every second. The interrupt request causes the MPU to execute the Mode Change Routine. A block diagram of the timer is shown in Figure 20. The timer consists of an eight-bit counter which is decremented toward zero by the f_{CIN} input. When the counter reaches zero, it sets the Timer Interrupt Request Bit (TIR) of the Timer Control Register (TCR), and a timer interrupt request is generated unless the

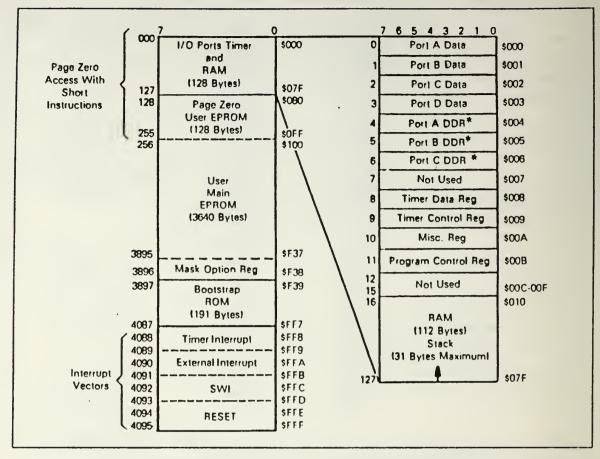


Figure 19. MC68705U3 Memory Configuration: From Ref. 10: p. 5.

Timer Interrupt Mask Bit (TIM) of the TCR is set. A brief description of each of the timer registers and their configuration follows.

- (1) Timer Data Register (TDR). The TDR is the eight-bit counter which sets the TIR bit of the TCR when it decrements to zero.
- (2) Timer Control Register. The contents of the TCR determine the general operation of the timer.
 - Bit 7, Timer Interrupt Request (TIR), signals a TDR underflow when it is set and will cause a timer interrupt request if the TIM bit of the TCR is clear. The TIR is cleared by the MPU reset or by program control.
 - Bit 6, Timer Interrupt Mask (TIM), inhibits a timer interrupt request when it is set. It is set by external reset or program control to inhibit the Blinking Mode, and is cleared by software when the Blinking Mode is requested by the operator.
 - Bit 5, External or Internal Clock Select (TIN), is used to select the timer clock source. Since the internal clock is used in this application, the TIN bits of both

Table 3. MPU CONNECTIONS

Pin	Name	Description					
1	V _{SS}	Ground					
2	RESET	When RESET is pulled low program execution halts, all variables are reinitialized and the Pan display is set to zero. SW1(P) controls the RESET line on the Pan MPU.					
3	ĪNT	Allows asynchronous interruption of the processor. When INT is pulled low by the Count Edge Detector the MPU executes the "Count Routine".					
4	V _{cc}	+ 5 V dc power connection.					
5	EXTAL	External clock input. Connected to a 4.0 MHz external clock which provides the MPU system clock.					
6	XTAL	Crystal clock input. Connected to ground since an external clock is used.					
7	V_{PP}	Programming voltage pin. Connected to V_{cc} for normal operation.					
8	Timer	External timer control input. Connected to V_{cc} since the internal timer is used.					
	Port C	General Purpose I/O lines.					
9	PC0	The two least significant digits in the display are represented in bi-					
10	PC1	nary coded decimal (BCD) by these eight lines.					
11	PC2						
12	PC3						
13	PC4						
14	PC5						
15	PC6						
16	PC7						
	Port D	General Purpose input lines.					
17	PD7	PD7 is the Channel A input to the MPU.					
18	PD6' INT2	PD6 is used as a second interrupt line. When PD6 goes low the MPU changes display modes.					
19	PD5	PD5 is the Channel B input into the MPU.					
20	PD4	PD4 is the Function input into the MPU.					
21	PD3	PD3 is the Set input into the MPU.					
22	PD2	PD2-PD0 are not used and are tied to ground.					
23	PD1						
24	PD0						

Table 4. MPU CONNECTIONS (CONT'D.)

Pin	Name	Description				
	Port B	General Purpose I'O lines (LED compatible).				
25	PB0	The most significant digit is represented in BCD by PB0-PB3 except				
26	PB1	on the Tilt MPU where these lines are connected to ground.				
27	PB2	PB4 determines which digits in the display are blanked.				
28	PB3	PB5 is not used. Connected to ground.				
29	PB4	PB6 determines the presence or absence of the display minus sign.				
30	PB5	PB7 determines the presence or absence of the display decimal point.				
31	PB6					
32	PB7					
	Port A	General Purpose I, O lines.				
33	PA0	The third and fourth least significant digits are represented in BCD				
34	PA1	by these eight lines.				
35	PA2					
36	PA3					
37	PA4					
38	PA5					
39	PA6					
40	PA7					

MPU's are always cleared. For the same reason the Timer pins are connected to V_{CC} (see Table 3).

- Bit 4, External Enable (TEE), is not used by the measurement system. By keeping the TEE clear at all times, the 68705's internal timer is used exclusively.
- Bit 3, Prescaler Clear (PSC), is not used in this application; always cleared.
- Bits 2-0, Prescaler Select (PS2, PS1 and PS0), are always set during program execution. This causes the internal timer signal frequency to be divided by 128.
- (3) Mask Option Register (MOR). Unlike the TDR and TCR the MOR is not software programmable; instead, it is implemented in EPROM.
 - Bit 7, the Clock bit, is cleared to allow operation of the external 4.0 MHz clock.
 - The Timer Option bit (TOPT), bit 6, is also cleared in this application. This permits the TCR to be software programmable.
 - Bit 5 is cleared to permit the use of the internal clock with the timer.
 - Bits 4 and 3 are not used.

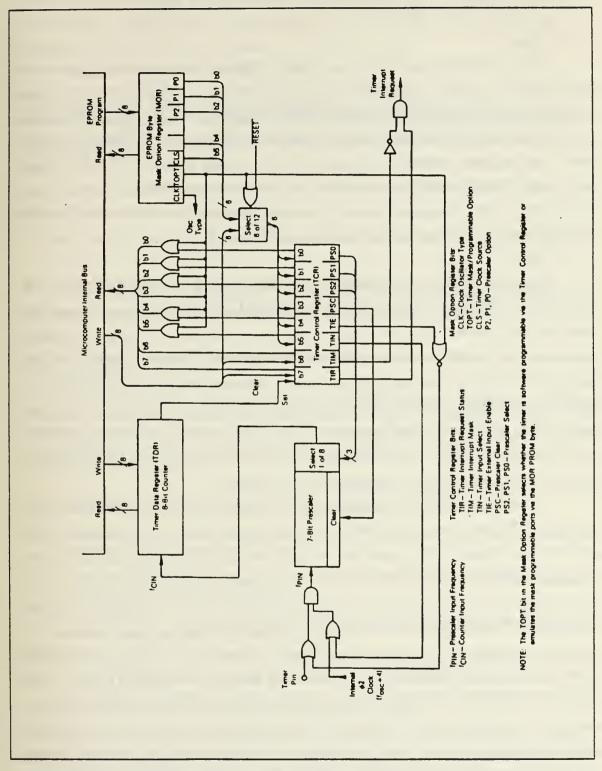


Figure 20. MC68705U3 Timer Functional Block Diagram.: From Ref. 10: p. 8.

• Bits 2-0 are all set and serve the same function as PS2, PS1 and PS0 bits of the TCR. [Ref. 10: pp. 6-8, 13-15]

3. RAM

The MC68705U3 has 112 bytes of RAM. The 112 bytes includes 31 bytes that can be used for the stack. Use of the stack is quite limited. During interrupts it is used to save the contents of the CPU registers and the program counter. During subroutine calls only the program counter is saved. The user's program has no other access to the stack. The programs written for each of the MPU's require less than 25% of the available RAM. The Pan MPU uses 27 of the 112 available bytes and the Tilt MPU uses only 22 bytes. The programs listed in Appendix D explain the function and give the location in memory for each of the variables. [Ref 10: p. 5]

4. ROM

The 3776 bytes of user EPROM in the MC68705U3 are divided into three separate blocks in the memory. Page Zero User EPROM is the ROM located between address S080 and S0FF. Because these addresses are only one byte long, instructions located in Page Zero ROM can be referenced with addressing modes not permitted with instructions located in other parts of the memory. Between address S100 and SF37 is the User Main EPROM. This portion of the memory in each MPU contains the vast majority of the signal conditioning programs. Located in another portion of the EPROM are the Interrupt Vectors. In each of these locations is the address of the first instruction the MPU is to execute when a particular interrupt occurs.

As with the RAM only a fraction of the available EPROM has been used in this application. The Pan MPU uses 899 bytes of the 3776 available and the Tilt MPU uses only 767 bytes. Since both programs are so small, one could reasonably ask why the two programs were not both put in one MPU. The primary problem with this idea is that each microprocessor can perform only one operation at a time. As indicated at the end of Chapter II, if the camera servo is rotating about its vertical axis at its maximum velocity of 1 rpm, the Pan signal conditioner must be capable of counting and displaying 51,200 counts per minute. Using a 4.0 MHz clock this allows the MPU 1172µs to count each pulse. Similarly the Tilt MPU has 1758µs to count each pulse when the camera is rotating at its maximum velocity about the horizontal axis. Assuming that the camera is rotating at its maximum velocity on both axes at the same time, and one MPU is being used to count the pulses from both encoders, the MPU needs to count 76,800 pulses per minute, which only allows 781.3 µs per pulse. The Pan MPU currently requires a max-

imum of 1032 instruction cycles or $1032\mu s$ to count a single pulse, and the maximum execution time for a single pulse on the Tilt axis is $825\mu s$. Thus, a single 68705 lacks the computational speed required to ensure that no counts would be missed if it was used to process the data from both encoders.

5. Central Processing Unit (CPU)

The CPU of the M6805 Family is implemented independently from the I/O or memory configuration. Consequently it can be treated as an independent central processor communicating with I/O and memory via internal address, data and control buses. [Ref 10: p. 6]

The CPU has five registers that are available for use by the operator. The function of each of these is described below.

- The Accumulator (A) is a general purpose data register used for arithmetic calculation and data manipulation.
- The Index Register (X) can be used as a second accumulator but is generally used for the indexed addressing mode. In the indexed addressing mode an effective address is created by adding the contents of X to a number provided by the instruction.
- The Program Counter (PC) contains the memory address of the next instruction to be executed by the MPU.
- The five bits of the Condition Code Register (CCR) keep information concerning the results of the last instruction executed by the MPU. Reference 14 gives a detailed description of each of the instructions in the M6805 Family Instruction Set and explains the effect of each instruction on the CCR. A brief description of each bit in the CCR follows.
 - The Carry (C) bit is set if a carry or a borrow was generated by the last arithmetic instruction. The state of the C bit can be software controlled.
 - The Zero (Z) bit is set if the result of the last arithmetic, logic or data manipulation instruction was zero.
 - The Negative (N) bit is set if bit seven of the result of the last arithmetic, logic, or data manipulation instruction is set.
 - The Half Carry (H) bit is set if an ADD or an ADC instruction causes a carry to occur between bits 3 and 4 of the result.
 - The Interrupt Mask (I) bit is set when an external interrupt (INT) occurs. If another interrupt occurs (e.g. Timer Interrupt or INT2) when the I bit is set, the second interrupt is latched so that it can be processed as soon as the I bit is cleared. The I bit can be set or cleared by software.
- The contents of the Stack Pointer (SP) are the address of the next available location on the stack. As previously discussed, the stack is only used to keep track of the PC during subroutine branches, and all of the CPU registers during an interrupt. [Refs. 10: p. 6, 14: pp. 14-15]

6. Input

Each MPU uses six input lines. Two of these lines, INT and INT2, are interrupt lines that detect a negative-going edge on their respective lines. The other four lines are general purpose input lines on Port D. All of the pins on Port D are TTL compatible which made the hardware design relatively straightforward. The electrical characteristics for the input pins are listed on p. 2 of Ref. 10.

The general operation of the two interrupt lines is described in Table 3 on page 39. Once they are understood, interrupts are a simple yet powerful tool. Only three of the four interrupts available on the MC68705U3 are used by the Pan and Tilt programs. The software interrupt is not used. When the MPU is interrupted, current program execution is halted, the contents of the CPU registers are placed on the stack, and the MPU fetches the contents of the appropriate interrupt vector from memory. After the interrupt vector has been fetched, the PC is moved to that address and execution of the interrupt routine begins. There is no ambiguity when an external interrupt occurs since there is a dedicated interrupt vector in memory. The timer interrupt and $\overline{\text{INT}}$ however share the Timer Interrupt Vector. When one of these interrupts occurs, the interrupt routine must determine the source of the interrupt by checking the TIR bit of the TCR and bit 7 of the MR to determine the source of the interrupt [Ref. 10: p. 11]. Normal program execution resumes at the point at which the interrupt occurred when the interrupt routine executes a return from interrupt (RTI) instruction.

The Function and Set lines on pins 20 and 21 are connected to the Function and Set switches. The operation of these switches is described in Table 2 on page 36. The remaining two input lines to each MPU are Channels A and B from the respective shaft encoders. The MPU programs use the information from these two inputs to determine the direction of rotation and to identify repeated oscillations about a single transition.

7. Output

Each MPU is designed to provide position information at its output in two basic forms. On the Pan axis, in the Count Mode a number between -51,200 and \pm 51,200 constitutes the output while in the Position Mode the output is an angle between 0° and 360°. A five digit display with a minus sign is sufficient for the count display. Using a five digit display with a decimal point in the Position Mode permits the angle to be displayed to the nearest hundredth of a degree. This resolution is not quite as good as the resolution of the shaft encoders (\pm 0.007°); however, final testing of the measurement system revealed that resolution is actually limited to about \pm 0.02° on the Pan axis and

about $\pm 0.14^{\circ}$ on the Tilt axis. The five digit display is therefore completely adequate for this system.

The Pan MPU uses 23 of its 24 output pins to represent the five digits, a minus sign and a decimal point. Each of the five digits is available in BCD form on four output pins of the MPU. The five digits are referred to as Digit 1, Digit 2, etc., with Digit 1 being the least significant digit and Digit 5 being the most significant digit. Port A has as its output the BCD representation of Digit 3 and Digit 4. Digit 1 and Digit 2 are represented by the output of Port C. The low four bits of Port B contain the BCD representation of Digit 5. These 20 output lines are the input to five 74LS47, BCD/7-Segment Decoder/Drivers, which decode the BCD signals and drive the common anode LED indicators. The output from Pin 29, PB4, is one input to a 74LS32 OR gate, the output of which is used to blank leading zeros out of the display. Pin 30 is not used and is tied to ground. The remaining two output pins drive two LED segments in the display. The signal on pin 31 turns the minus sign off and on, and the signal on pin 32 determines whether the decimal point is displayed.

The electrical characteristics of the I₁O Ports are given on p. 4 of Ref. 10. The output characteristics of Ports A₂ B and C are compatible with the input characteristics of the 74LS47 and the 74LS32 given on pp. 4-59 and 4-48 of Ref. 11. The pins on Port B are capable of sinking 10 mA when Port B is configured as an output port. A 220 Ω resistor placed in series with each of the display segments limits the current to approximately 9 mA and permits the MPU to drive the decimal point and minus sign directly.

One consideration in the design of this system was to provide a system capable of being readily expanded to meet changing needs. To this end, in addition to being connected to the LED display devices via the 74LS47's, the BCD data lines are also connected to a header on each of the MPU circuit boards. If, at a later date, the position information needs to be used in another system, a jumper connected to each of the headers could provide the information with little or no modification.

The Pan and Tilt signal processing subsystems are virtually identical in the hardware used to implement them. The only difference is that the Pan system has a five digit display, and the Tilt system needs only four digits to display its position information. Consequently, the Tilt system does not use Digit 5, and pins 25-29 are tied to ground.

F. DISPLAY

Each digit represented in BCD at the output of the MPU is decoded by a 74LS47 BCD/7-Segment Decoder/Driver. The decoding devices each convert a four bit BCD representation of a number into seven signals that each drive a separate segment of a common anode, seven segment, LED display. The 74LS47 is capable of sinking 24 mA from each of the LED segments. Without a current limiting resistor between each of the output pins on the 7447 and the corresponding pin on the display element however, this maximum current is exceeded. When this happens the LED's have a very short life, the 7447 overheats and the system fails to function properly. The addition of a 220 Ω resistor in each branch limits the current to about 9 mA per segment, and permits trouble-free operation.

Three of the output pins on each MPU are not used as inputs to the 7447's. As discussed in the previous section, the Decimal and Minus lines each drive individual LED segments directly. The third line, also mentioned briefly in the preceding section, is used with the Blanking In/Ribbon Blanking Out (BI/RBO) signal from Digit 4's 7447 to determine the Ribbon Blanking In (RB1) signal into the 7447 which drives the display for Digit 3.

The term "blanking" simply means removing the leading zeros from the display. The two display modes available from the MPU's have different blanking requirements. In the Position Mode the three least significant digits are not blanked, while in the Count Mode, all but the least significant digit are blanked. The RBI and BI/RBO pins on the 7447's, the Blank line out of each MPU and the OR gates, connected as shown in the schematics in Appendix A, provide this capability.

The Light Test (LT) pin on each 7447 is connected to SW5. When the switch is closed, the Light Test line goes low and each of the output lines on each of the 7447's also goes low, thus sinking current from all of the LED segments simultaneously. This feature allows the operator to check for inoperable display segments.

G. POWER SUPPLIES

The two power supplies shown in Figure 2 on page 6 are each +5.0 Vdc supplies. The power supply which provides power to the shaft encoders and the line drivers is physically mounted in the camera housing. It was built by modifying the +12 Vdc auto iris power supply. This was accomplished using an LM7805 Voltage Regulator in the manner shown in Figure 8 of Appendix A. The auto iris requires only 100 mA at +12 Vdc for correct operation, and the LM7812 Voltage Regulator has an available

output current of 1.0 A [Refs. 15, 16]. The remaining 900 mA is available to the LM7805 to power the encoders and the line drivers. Reference 9 lists the maximum power requirement for the HEDS-600 as 40 mA at +5 Vdc, and Ref. 11 specifies the maximum power requirement for a 74S140 is 1 mA at +5 Vdc. Thus, the 84 mA requirement for the two encoders and four line drivers is well within the capabilities of the modified power supply.

The second power supply is capable of providing 6.0 A at +5 Vdc which is more than adequate to provide the 1.4 A needed by the signal processors and the display devices. The power supply also has 12 Vdc and -5 Vdc ports. To preclude the potentially disastrous results which might occur if the power supply were incorrectly connected to the signal processor/display devices, the circuitry shown in Figure 21 was included on each MPU and display printed circuit board.

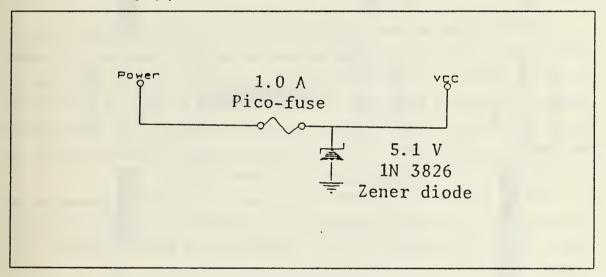


Figure 21. Reverse/Over-voltage Protection Circuit

IV. CALIBRATION, TESTING AND IMPLEMENTATION

A. GENERAL

Once the basic system design had been completed, and the MPU programs had been written, a prototype system was constructed. The prototype system might also be called the development model, since it was not only used to test the design, but was also used to calibrate the MPU programs. A block diagram of the prototype system is shown in Figure 22. The M68705EVM Evaluation Module (subsequently referred to as the EVM) provided the capability to debug and evaluate the MC68705U3-based signal processing subsystem. Operation of the signal processing MPU was performed by an MC68705U3 resident on the EVM.

The prototype system provided considerable flexibility in the testing and calibration of the system. The assembly language programs for the MPU's were written and edited on the PC. They were then assembled and linked using the 2500 A.D. 6805 Cross Assembler and 2500 A.D. Linker [Ref. 17: pp. (1-1)-(2-38)]. The result, a Motorola S19 output file (see [Ref. 17: pp. (A-1)-(A-4)]), was then down-loaded to the EVM using the file transfer program, Kermit. Downloading procedures are detailed in [Ref. 18: pp. (3-10)-(3-25),(3-37)]. The PC-EVM interface is shown in Figure 23.

After the program had been down-loaded into the MC68705U3 resident on the EVM, data entry and program debugging were controlled via the CRT monitor keyboard. The CRT-EVM interconnection is shown in Figure 24 and the monitor commands are described in [Ref. 18: pp. (3-8)-(3-25)].

The remainder of the signal processing functions were realized using hardware external to the EVM. These functions included edge detection of the output signals from the shaft encoders, decoding the output of the MPU, and generating the signals to drive the display devices. This portion of the prototype, referred to by [Ref. 18] as the "target system", was built on breadboards and is represented by the block in the center of Figure 22. The target system was connected to the MCU via a 40-pin jumper header, J1, on the EVM. The pinout for J1 is shown in Figure 25. The labels in Figure 25 refer to the labels used in the schematic diagrams which are shown in Appendix A.

B. CALIBRATION

Once the MPU programs were capable of counting the pulses generated by the shaft encoders, the programs needed to be "calibrated". This calibration procedure required

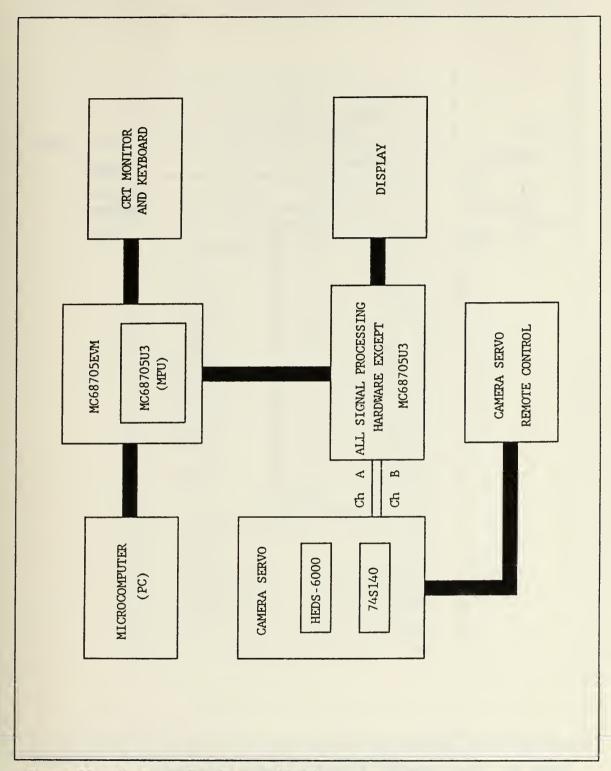


Figure 22. Prototype/Development Model

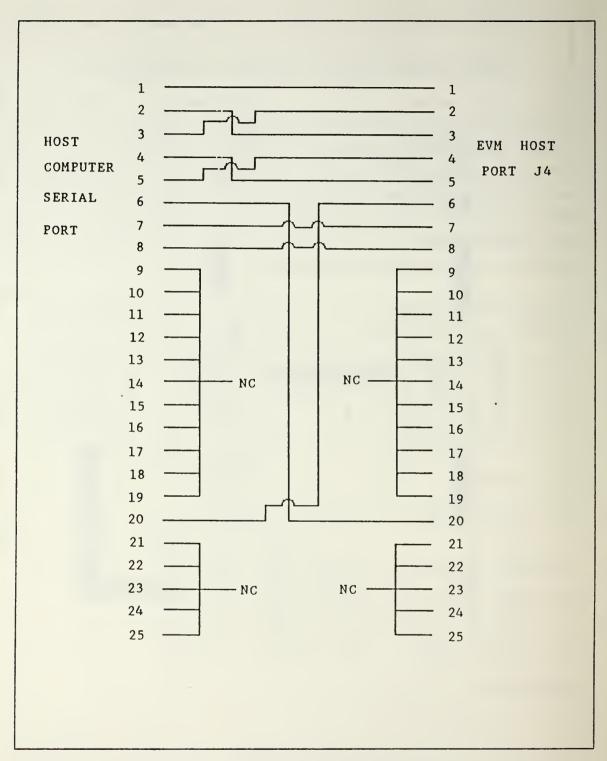


Figure 23. Host Computer - Evaluation Module Connections

	1	. 1		
	2	. 2		
	3	3		
CRT	4	 4	EVM	
TERMINAL	5	. 5		
PRIMARY	6	. 6	TERMINAL	
PORT	7	 7	PORT J3	
	8	 . 8		
	9	. 9		
	10	. 10		
	11	- 11		
	12	. 12		
	13	. 13		
	14	. 14		
	15	15		
	16	16		
	17	. 17		
	18	 . 18		
	19	19		
	20	 20		
	21	. 21		
	22	. 22		
	23	 23		
		24		
	25			
	23	23		

Figure 24. Monitor - Evaluation Module Connections

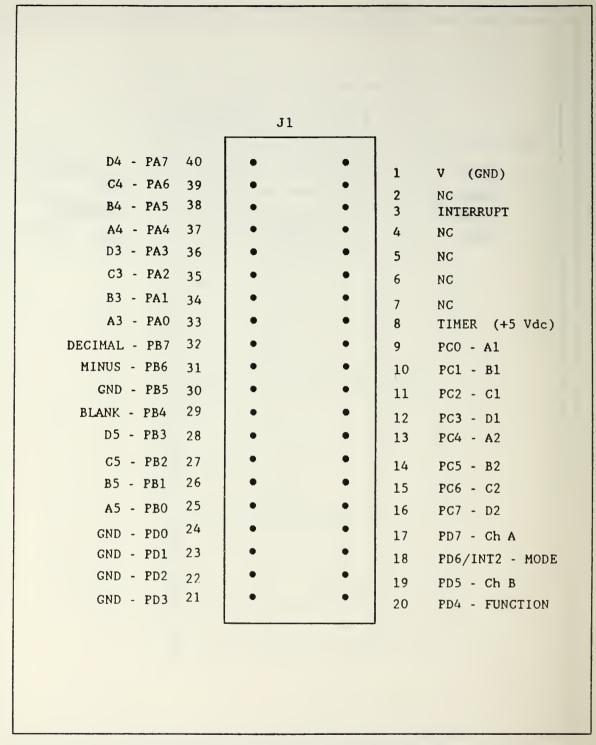


Figure 25. Evaluation Module - Signal Processor Connections

determining the angular distance through which the camera rotated between successive pulses from the shaft encoder. This number is a scale factor, which, when multiplied by the total number of pulses from the shaft encoder, yields a number equal to the angular displacement of the camera. The calibration procedure also involved determining the amount of hysteresis present in each of the gear trains.

1. Scale Factor

To determine the scale factor (SF) the simple geometric relationship

$$\theta = \tan^{-1} \left(\frac{\text{opposite}}{\text{adjacent}} \right)$$
 (12)

was used. Using a small laser attached to the camera servo, and the geometry shown in Figure 26, the SF could be experimentally determined. As the camera servo was rotated through an angle, θ , the MPU was used to count the output pulses from the shaft encoder. The laser beam was projected on a vertical surface at a distance, a, away from the axis of rotation. The beam of the laser spread to a diameter of approximately 0.4 in. over a distance of 30 ft. A template with a 0.4 in. diameter aperture was used to mark the location of the "spots" on the distant wall. The distance between the spots, l, was measured by selecting one edge of one of the marks and measuring the distance to the corresponding edge of the distant mark. Then, having determined l and a and reading the count, C, from the display, the SF could then be determined from

$$SF(degrees/Pulse) = \frac{\theta}{C}$$

$$= \frac{\tan^{-1}\left(\frac{l(in)}{a(in)}\right)}{C}.$$
(13)

Using Equation (13) to simplify the expression,

$$d(SF) = \frac{\delta(SF)}{\delta l} dl + \frac{\delta(SF)}{\delta a} da$$
 (14)

yields

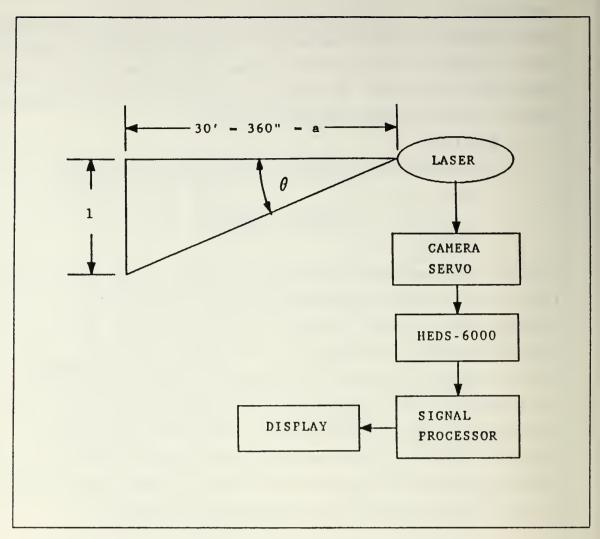


Figure 26. Geometry Used to Determine the Scale Factor

$$d(SF) = \frac{1}{C} \frac{\delta \theta}{\delta l} + \frac{1}{C} \frac{\delta \theta}{\delta a} da$$

$$= \frac{1}{C} \left(\frac{a}{a^2 + l^2} \right) dl + \frac{1}{C} \left(-\frac{l}{a^2 + l^2} \right) da$$

$$d(SF) = \frac{(adl - lda)}{C(a^2 + l^2)},$$
(15)

which indicates that C, a and l should all be as large as possible to minimize the error in SF due to a measurement error in a or l. The physical size of the laboratory limited the distance, a, to 30 ft. When a = 30 ft, l was limited to about 3.5 ft in the horizontal

plane and about 4.0 ft in the vertical plane. By modifying the geometry as shown in Figure 27, the count, which from Equation (13) is directly proportional to θ , could also be maximized. The configuration shown in Figure 27 was used to obtain the scale factor calibration data for the Pan axis. However, since the servo is incapable of rotating 360° about the Tilt axis, the test configuration shown in Figure 26 had to be used the collect the data for that axis.

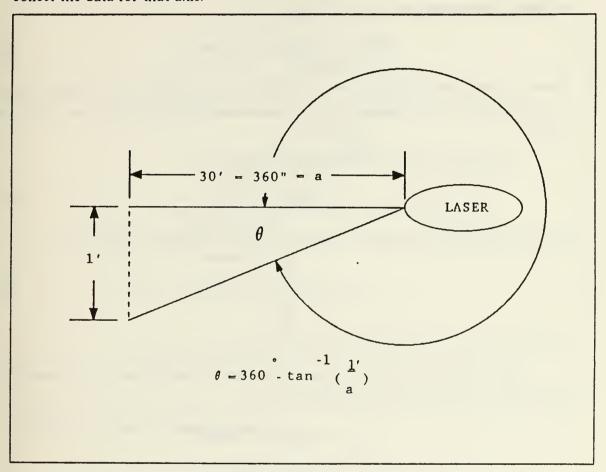


Figure 27. Alternate Geometry Used to Determine the Scale Factor

Adopting the notation, \overline{X} , to represent the mean value of a random variable, X; if X is discrete with N measured values,

$$\overline{X} \simeq \frac{1}{N} \sum_{l=1}^{N} X_{l} \tag{16}$$

where X_i is the *i*th measured value of X, and the approximation becomes better as N approaches infinity.

Using the expression in Equation (16) and the measured data for the scale factors, from 31 measurements on the Pan axis,

$$\overline{SF}_{Pan} = (7.0312 \times 10^{-3})^{\circ} Pulse^{-1}$$
, (17)

and after 32 measurements on the Tilt axis,

$$\overline{SF}_{Tilt} = (7.0452 \times 10^{-3})^{\circ} Pulse^{-1}$$
, (18)

where the subscripts indicate the axis. The actual implementation of these scale factors is described later in this chapter and in the documentation for each of the MPU programs.

If the error in the ith measurement is described by

$$e_i = X_i - \overline{X} , \qquad (19)$$

then the root mean square (RMS) error in N measurements of X is given by;

$$\sigma_{\mathbf{x}} = \sqrt{\frac{1}{N}} \sum_{l=1}^{N} (X_l - \overline{\mathbf{X}})^2 \quad . \tag{20}$$

Note that this is also the definition of the standard deviation of X.

The RMS errors in the Pan and Tilt scale factor measurements were determined from Equation (20) and the measured data to be;

$$\sigma_{\rm SF_{\rm Pan}} = (4.62 \times 10^{-6})^{\circ} \rm Pulse^{-1}$$
 (21)

$$\sigma_{\rm SF_{Tut}} = (6.89 \times 10^{-6})^{\circ} \, \rm Pulse^{-1} \ .$$
 (22)

As before, the subscripts are used to identify the axis and the source of the error. The fact that the errors are small compared to the mean values suggests that the means should closely approximate the actual values for the scale factors.

2. Hysteresis

Houghton defines backlash in wormgearing as "...the total play between the surfaces of the worm and worm wheel teeth measured normal to the faces." [Ref. 19: pp. 1.4, 1.5] Backlash only poses a problem in the measurement system when the servo's

direction of rotation changes. Figure 28 is a typical hysteresis curve. As long as the direction of rotation of the worm is increasing the $\theta_{\text{WORM}}/\theta_{\text{WORMGEAR}}$ relationship is linear. However, when the direction of rotation reverses there is a region, depicted by the left pointing arrows, where the position of the worm changes without a corresponding change in the position of the wormgear. Note that once all of the backlash has been taken up the $\theta_{\text{WORM}}/\theta_{\text{WORMGEAR}}$ relationship is again linear until the direction of rotation changes.

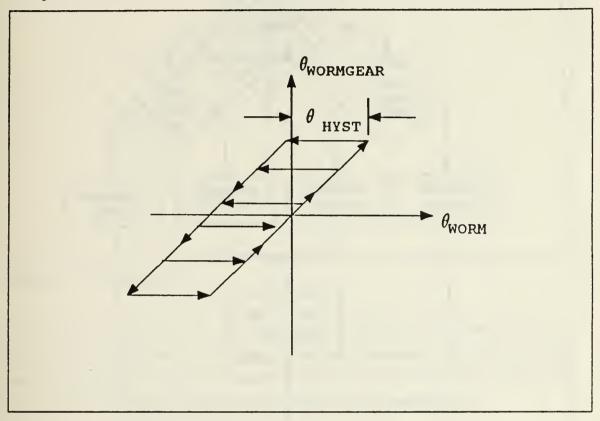


Figure 28. Typical Hysteresis Curve

The purpose of the hysteresis buffer in the MPU is to permit the signal processor to account for the backlash error introduced into the measurement by the worm-wormgear connection. The theory of operation for the buffer is relatively straight forward and is best described by the flow diagram in Figure 29. The buffer is a data byte in the MPU RAM. As long as the buffer is full, i.e., the contents are equal to the predetermined buffer length, a clockwise (CW) signal from the shaft encoder (increasing elevation and increasing azimuth are defined as CW rotation for the purposes of this system) causes the position counter to be incremented. Similarly, counter-clockwise

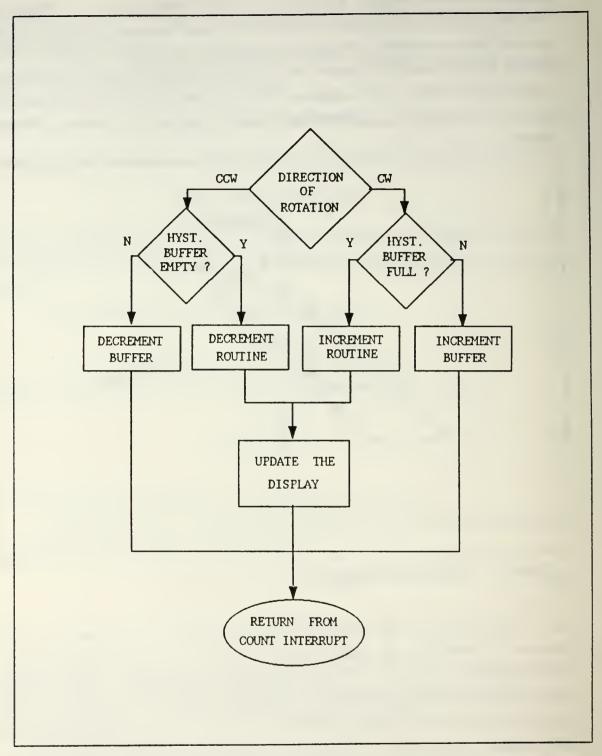


Figure 29. Operation of the Hysteresis Buffer

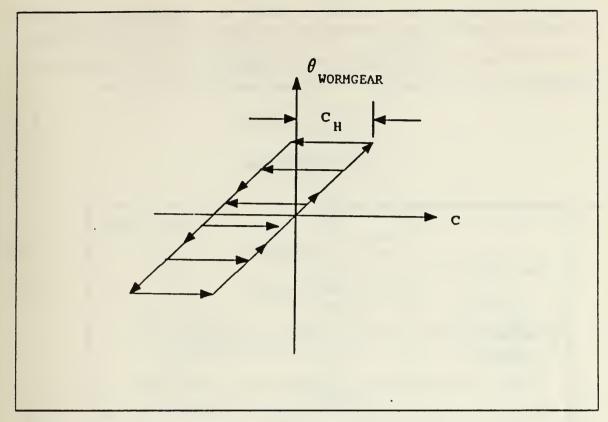


Figure 30. Hysteresis Curve

(CCW) signals cause the position counter to be decremented if the hysteresis buffer is empty, i.e., the contents are equal to zero. These two situations correspond to the two linear sections in Figure 28. From Equation (13), the horizontal separation of these two lines is related to the length of the hysteresis buffer, C_H by the expression

$$C_{H} = \frac{\Delta \theta_{H}}{SF} \quad . \tag{23}$$

Similarly, using the \overline{SF} to map θ_{WORM} into C, and the fact that the displacement of the wormgear equals the displacement of the axis of interest, the curve shown in Figure 30 can be obtained from Figure 28. From Figure 30 it is apparent that two different pulse counts can be obtained for any given position, θ , depending on whether that position is approached from a CW or a CCW direction. The difference in the two counts is a measure of the hysteresis present in the gear train and is also the required length for the hysteresis buffer. By using this difference as the length of the hysteresis buffer, counts received by the MPU which occur while the gears are operating on one of the horizontal

sections of the curve in Figure 30 are not considered "valid" and therefore do not cause the MPU to modify the position. Using Equation (23) and data collected in the laboratory the average hysteresis present in each of the gear trains was determined (from 45 measurements on the Pan axis and 30 measurements on the Tilt axis) to be

$$\overline{C}_{H(Pan)} = 7.39 \text{ Pulses}$$
 (24)

$$\overline{C}_{H(Tilt)} = 6.06 \text{ Pulses}$$
 (25)

and the RMS errors were calculated to be,

$$\sigma_{C_{H(Pan)}} = 1.0 \text{ Pulses} \tag{26}$$

$$\sigma_{C_{\text{H(Tilt)}}} = 0.91 \text{ Pulses}$$
 (27)

C. IMPLEMENTATION OF THE CALIBRATION DATA

1. Background

Figure 31 outlines the basic operation of each of the MPU's. Although each of the routines is described in detail by the comments included in the programs, the operation of the Count Routine is the heart of the program and should be explained prior to discussing the actual implementation of the experimental results.

When the system operator causes the camera servo to rotate, each optical shaft encoder translates the displacement of one of the axes into two series of digital pulses. The two pulse trains, referred to as Channels A and B, are TTL logic level signals. When the logic level of Channel A transitions from low to high (rising edge transition) or from high to low (falling edge transition), the edge detector (See Figure 15 on page 33) pulls pin 3 of the associated MPU low for approximately 2 μ sec. When this occurs an external interrupt (EXT INT or $\overline{\text{INT}}$) request is generated and the MPU begins execution of the Count Routine.

As mentioned in Chapter III, since both rising and falling edge transitions are detected by the edge detector, the signal processor must be capable of detecting multiple oscillations of the shaft about a single logic level transition point. Accordingly, the first tasks performed by the Count Routine are to determine the direction of rotation and to simultaneously determine whether the interrupt is the result of a stationary shaft oscillation. To do this the Count Routine checks the state of pin 17 (Channel A) and pin 19 (Channel B). Operation of this portion of the routine is summarized in Table 5.

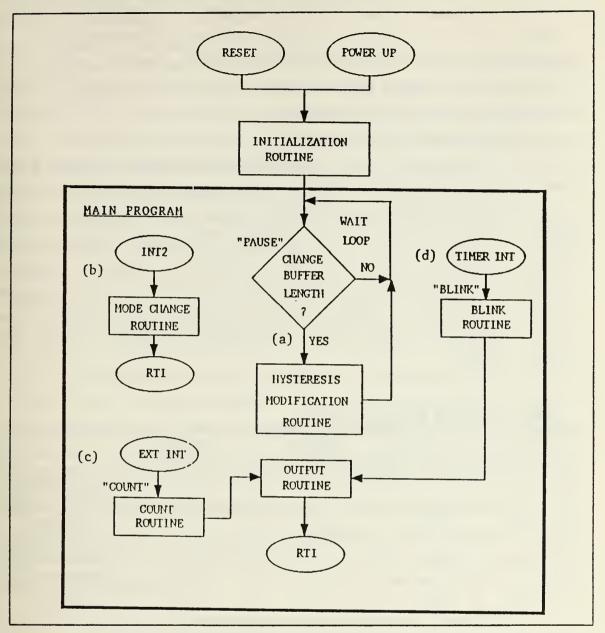


Figure 31. Program Flow Diagram: Program executes in the Wait Loop until; (a) the operator requests to modify the hysteresis buffer, (b) the operator requests to change the display mode, (c) an external interrupt is generated by the Channel A edge detector or, (d) a timer interrupt causes the display mode to "blink". All interrupt routines are terminated with a return from interrupt (RTI) command.

Note that CW rotation is indicated when Channel B leads Channel A in phase and CCW rotation is indicated if Channel A is leading Channel B. The possibility of erroneously counting multiple oscillations about a single point is eliminated by "counting" only the leading edge transitions when the shaft is rotating CW and only the trailing edge transitions when the rotation is CCW. All other transitions cause the program to execute a "return from interrupt" (RTI) instruction.

2. Implementing the Hysteresis Buffer

The transitions that are to be counted cause the program to compare the contents of the hysteresis buffer, HYSTCT, and the direction of rotation to the experimentally determined buffer length, HYST $\simeq \overline{C}_H$. If the rotation is CW and the buffer is full (i.e., HYSTCT=HYST), or if the rotation is CCW and the buffer is empty (i.e., HYSTCT=0), then the "slack" due to the gear backlash should have been taken up, the transitions are considered "valid" and the MPU modifies the position appropriately. "Invalid" counts cause the contents of the hysteresis buffer to be incremented or decremented depending on whether the present direction of rotation is CW or CCW (Figure 29 refers).

Table 5. COUNT ROUTINE LOGIC

Channel A	Channel B	Direction of Rotation	Count the Pulse?	Action
Low	Low	CW	No	Increment the hysteresis buffer.
Low	High	CCW	Yes	Decrement the position.
High	Low	CCW	No	Decrement the hysteresis busser.
High	High	CW	Yes	Increment the position.

From the calibration data for the Pan axis, $\overline{C}_{H(Pan)} \simeq 7.4$ and $\sigma_{C_{H(Pan)}} \simeq 1.0$. Because the length of the hysteresis buffer must be an integer value, $\overline{C}_{H(Pan)}$, needed to be rounded off. Rounding to the nearest whole number initially seemed the most logical approach. Upon further consideration, however, it was decided to round 7.4 up to 8. Considering the relatively small data base (45 measurements) upon which the average was based, the fact that the standard deviation was 1.0 and that the gear backlash will only increase

with time, this seemed like the most reasonable approach. The buffer length for the Tilt axis was set equal to $6(\overline{C}_{H(T)} = 6.06)$.

3. Implementing the Scale Factor

There are three counters in each MPU that keep track of the position information for the axis of interest. The first, BINCT, is simply a binary counter that is incremented by one for each valid CW count and decremented by one for each valid CCW count. The other two counters consist of two sets of pointers, two sets of data registers and a shared data table. Each byte in a pointer points to an address in the table that contains two BCD digits which make up a portion of the position information.

In order to increment (decrement) the pulse count, BCDCT, by one, the count pointer, CTPTR, is incremented (decremented) by one causing it to point to a new table address. The contents of the table at the new addresses are then moved into BCDCT. Modification of the position counter, DEGRES, is performed in much the same manner. DEGRES contains a BCD number that, when multiplied by 0.001, represents the angular position (in degrees) of the shaft of interest. Thus, each time the camera is displaced in a CW direction through one degree, the contents of DEGRES should be incremented by 1000. To do this, the position pointer, PTR, must be incremented (decremented) by seven or eight each time CTPTR is incremented (decremented) by one. Incrementing PTR by seven corresponds to an angular displacement of 0.007° and since \overline{SF}_{Pan} and \overline{SF}_{Tilt} are each slightly larger than 0.007° , periodically PTR must be incremented by eight to reduce the cumulative round off error. Specifically, if PTR is incremented by seven each time a valid CW pulse is detected (except when BINCT is an even multiple of 32) and is incremented by eight when BINCT is a modulo 32 number, the effective scale factor is given by:

$$SF_{eff_1} = \frac{1}{32} (31(0.007) + 0.008)$$

= 0.00703125°Pulse⁻¹, (28)

which is slightly larger than the desired 0.0070312° Pulse⁻¹, for the Pan axis and slightly smaller than the desired 0.0070452° Pulse⁻¹ for the Tilt axis. To further reduce the cumulative round off on the Pan axis, every 16,384 ($2^{14} = 32 \times 512$) counts PTR is incremented by seven instead of eight. This results in an effective scale factor of,

$$SF_{eff_2} = \frac{1}{512} \left\{ 511 \left[\frac{1}{32} (31(7) + 8) \times 10^{-3} \right] + 0.007 \right\}$$

= (7.03119×10^{-3}) °Pulse⁻¹, (29)

which is within two parts in one million.

The maximum error introduced into the measurement should occur when the camera is rotated through the largest possible angle. To predict this error on the Pan axis, when the camera has been displaced by 360°,

$$BCDCT = \frac{360^{\circ}}{\overline{SF}_{Pan}}$$
= 51,200 Pulses (30)

so the position error using SF_{eff_1} and SF_{eff_2} should be;

$$e_{Pan} = 360^{\circ} - [3(SF_{eff_2}) + (51,200 - 3(16,384))(S_{eff_1})]$$

= 0.00295°. (31)

Thus, the error due to the scale factor on the Pan axis should be well within the desired resolution of $\pm 0.006^{\circ}$.

Using SF_{ω_1} alone as the scale factor for the Tilt axis, the maximum theoretical error over $\pm 12^{\circ}$ due to the scale factor round off is determined in the same manner.

$$BCDCT = \frac{12^{\circ}}{\overline{SF}_{Tilt}}$$
= 17,033 Pulses (32)

So that,

$$e_{Tilt} = 12^{\circ} - 17,033(SF_{eff_1})$$

= 0.0234°. (33)

which again is significantly less than the required resolution of $\pm 0.23^{\circ}$ for the Tilt axis.

The final step in the Count Routine is a branch to the Display Routine. Depending on whether the MPU is in the Count or Position Mode, the Display Routine copies the contents of BCDCT or DEGRES to the output ports and then executes an RTI instruction.

D. FINAL TESTING

1. General

Final laboratory testing and evaluation of the measurement system was performed after the calibration results had been implemented in each of the MPU Count Routines. The purpose of the testing was to verify that the calibration results had been properly coded into the MPU's and to determine the resolution capabilities of the measurement system experimentally.

This verification process included determining the combined error due to the hysteresis and scale factor errors. The use of some simple multiple random variable theory was therefore required. From [Ref. 20: pp. 121,122] the variance of a weighted sum of M random variables is the weighted sum of their covariances, C_{x,x_j} , and is given by,

$$\sigma^2 = \sum_{i=1}^{M} \sum_{j=1}^{M} \alpha_i \alpha_j C_{X_i X_j} , \qquad (34)$$

where α_i is the weight associated with X_i . Additionally, the covariance can be expressed as

$$C_{XY} = \rho \sigma_X \sigma_Y \quad , \tag{35}$$

where ρ is the normalized second-order moment and is known as the correlation coefficient of X and Y. The correlation coefficient is bounded by

$$-1 \le \rho \le 1 . \tag{36}$$

In the case where there are two equally weighted random variables, M = 2 and $\alpha_i = \alpha_j = 1.0$. Substituting into Equation (34) and expanding

$$\sigma^2 = C_{XX} + C_{XY} + C_{YX} + C_{YY} . \tag{37}$$

Using Equation (35),

$$\sigma^2 = \sigma_X^2 + 2\rho\sigma_X\sigma_Y + \sigma_Y^2 . \tag{38}$$

Combining (36) and (38) yields

$$\sigma_X^2 - 2\sigma_X\sigma_Y + \sigma_Y^2 \le \sigma^2 \le \sigma_X^2 + 2\sigma_X\sigma_Y + \sigma_Y^2 . \tag{39}$$

The bounds of the combined scale factor and hysteresis errors can therefore be determined from

$$\sqrt{\sigma_{e_{\rm SF}}^2 - 2\sigma_{e_{\rm SF}}\sigma_{e_{\rm H}} + \sigma_{e_{\rm H}}^2} \le \sigma_e \le \sqrt{\sigma_{e_{\rm SF}}^2 + 2\sigma_{e_{\rm SF}}\sigma_{e_{\rm H}} + \sigma_{e_{\rm H}}^2} . \tag{40}$$

where:

- σ_{\bullet} = standard deviation of the combined error,
- $\sigma_{e_{SF}}$ = standard deviation of the scale factor error, and
- σ_{e_H} = standard deviation of the hysteresis error.

Note that the bounds are determined by the two cases where the hysteresis error, e_H , and the scale factor error, e_{SF} , are "completely correlated". The upper bound corresponds to the case where an increase in e_{SF} implies an increase in e_H , and the lower bound corresponds to the case where an increase in e_{SF} directly implies a decrease in e_H .

A third case is also of particular interest. If e_H and e_{SF} are completely uncorrelated, i.e., $\rho = 0$, then from Equation (38),

$$\sigma_e = \sqrt{\sigma_{e_{\rm SF}}^2 + \sigma_{e_{\rm H}}^2} \quad . \tag{41}$$

which can also be written as

$$e = \pm \sqrt{e_{\rm SF}^2 + e_{\rm H}^2}$$
 , (42)

where $e=\pm\sigma_e$ is the 1.0 σ error due to the scale factor and hysteresis errors, e_{SF} and e_H respectively. Based on the physical nature of the two errors it is reasonable to assume that e_{SF} and e_H are statistically uncorrelated; however, no experimental data was collected to support this hypothesis. Due to this lack of a priori information, the maximum RMS error, $e_{max}=\pm\sigma_{e_{max}}$, given by

$$e_{\text{max}} = \pm \sqrt{e_{\text{SF}}^2 + 2e_{\text{SF}}e_{\text{H}} + e_{\text{H}}^2}$$
, (43)

will be used to describe the resolution capabilities of the measurement system.

2. Pan Axis

a. Hysteresis

To test the operation of the Pan axis hysteresis buffer, the Initialization Routine was programmed to set the buffer length to 8. Then, as described in the first section of this chapter, the servo was used to position the beam of a small laser on a fixed target. By approaching the target alternately from a CW and a CCW direction and

comparing the difference in the output counts from the shaft encoders, the hysteresis error was determined. The average error after 31 measurements was

$$\tilde{e}_{H(Pan)} = -0.1880 \text{ Pulses} , \qquad (44)$$

and the RMS error was

$$\sigma_{\mathbf{e}_{\mathbf{H}(\mathbf{Pan})}} = 1.7699 \text{ Pulses} . \tag{45}$$

Since the mean error is "near zero" compared to the standard deviation, the 1.0 σ error e_H , due to the hysteresis can be determined from

$$e_{H} = \pm \left(\sigma_{e_{H}}\right)\overline{SF} \tag{46}$$

so that

$$e_{H(Pan)} = \pm 0.0124^{\circ}$$
 (47)

b. Scale Factor

Verification of the scale factor was performed in the same manner as the scale factor calibration, except that the MPU was calibrated in the Count Mode and tested in the Position Mode. Since these tests sought to find the maximum error due to the scale factor, and the error is directly proportional to the angle that is being measured, these tests were conducted by displacing the camera servo through the maximum angles permitted by the camera and the laboratory. Specifically, on the Pan axis the servo was rotated through approximately 360°. The mean error due to the scale factor on the Pan axis was determined from 15 samples to be

$$\bar{e}_{SF(Pan)} = -0.0018^{\circ}$$
 (48)

and the RMS error was

$$\sigma_{e_{SF,Pan}} = 0.00890^{\circ}$$
 (49)

As with the hysteresis error, if we neglect the small bias due to the $\overline{e}_{SF(Pan)}$, we can describe the 1.0 σ RMS error due to the scale factor as

$$e_{SF(Pan)} = \pm \sigma_{SF(Pan)}$$

= $\pm 0.00890^{\circ}$ (59)

c. Combined Error

From Equation (42) the combined error on the Pan axis if e_H and e_{SF} are uncorrelated can be estimated as

$$e_{\text{Pan}} = \pm \sqrt{(0.0124)^2 + (0.0089)^2}$$

= \pm 0.01526°. (51)

And from Equation (43) the maximum combined error on the Pan axis is

$$e_{\text{Pan}_{\text{max}}} = \pm \sqrt{(0.0124)^2 + 2(0.0124)(0.0089) + (0.0089)^2}$$
 (52)

$$e_{Pan_{max}} = \pm 0.0213^{\circ}$$
 (53)

The combined error is approximately three times larger than the design specification limit and is due primarily to the hysteresis error.

3. Tilt Axis

a. Hysteresis

The procedure used to verify the operation of the calibrated Tilt MPU was identical to that described in the previous section. Using a hysteresis buffer length of 6 resulted in

$$\overline{e}_{H(Tilt)} = -0.0965 \text{ Pulses} \tag{54}$$

and,

$$\sigma_{e_{H(T,H)}} = 1.3156 \text{ Pulses} \tag{55}$$

after 13 samples. As before we can define the 1.0 σ error from $e = \sigma \overline{SF}$ to be

$$e_{H_{Tilt}} = \pm 0.00529^{\circ}$$
 (56)

b. Scale Factor

Testing the scale factor on the Tilt axis was limited by the physical construction of the servo and the size of the laboratory. The angle over which testing could be performed was limited to \pm 6° from the horizontal plane. Consequently, the RMS error for the scale factor on the Tilt axis was determined in exactly the same manner as

the RMS error for the Pan axis scale factor, but since the error due to rounding of the scale factor is directly proportional to the angle being measured the results were multiplied by 2.0 to account for the limited range of the test. The modified results should therefore be representative of the maximum error one should expect if the measurement system is used to measure elevation angles over a range of \pm 12°.

The error due to the scale factor is described from 16 samples by

$$\overline{e}_{SF(Tilt)} = 0.0070^{\circ} \tag{57}$$

and,

$$\sigma_{\mathsf{e}_{\mathsf{SF}(\mathsf{Tilt})}} = 0.0665^{\circ} \ . \tag{58}$$

Including the factor of two in the calculation we have

$$e_{SF(Tilt)} = \pm 2(0.0665^{\circ})$$

= $\pm 0.1330^{\circ}$. (59)

c. Combined Error

The combined RMS error is determined in the same manner as before. If e_H and e_{SF} are uncorrelated,

$$e_{\text{Tilt}} = \pm \sqrt{(0.1330)^2 + (0.00529)^2}$$

= 0.1331°,

and the maximum combined RMS error is

$$e_{\text{Tilt}_{\text{max}}} = \pm \sqrt{(0.1330)^2 + 2(0.1330)(0.00529) + (0.00529)^2}$$
 (61)

$$e_{Tilt_{max}} = \pm 0.1383^{\circ}$$
 (62)

The Tilt axis measurement system appears to perform well within the required resolution specifications.

E. FINAL IMPLEMENTATION

Once the program debugging, calibration and testing were completed, final implementation of the system remained. Taking the design from the prototype/development model to a fully functional system was a straightforward but time-consuming evolution.

The plans for the printed circuit boards (PCB's) were made directly from the schematics shown in Appendix A; the boards were then etched and assembled from the plans which are shown in Appendix B. All of this work was performed by sailors attached to the Academic Division of the NPS.

As previously discussed, the M68705EVM Evaluation Module provided a powerful and flexible means of debugging and evaluating the performance of the microprocessor based signal conditioner. Additionally, once program testing was completed the EVM's EPROM microprocessor programmer provided the means to program the EPROM MCU's. A detailed, but simple to follow, programming procedure for programming the MC68705U3 is given in [Ref. 18: pp. (3-26)-(3-27)].

V. CONCLUSIONS AND RECOMMENDATIONS

A. SYSTEM PERFORMANCE

The prototype system was calibrated and successfully tested in a laboratory environment. Experimental results indicate that the system is capable of measuring the video camera's elevation over a range of $\pm 12^{\circ}$ with a resolution of $\pm 0.138^{\circ}$ and its azimuth over 360° with a resolution of $\pm 0.021^{\circ}$. The system was designed to be low cost, reliable, and easy to operate. Only time will tell whether these objectives were truly achieved.

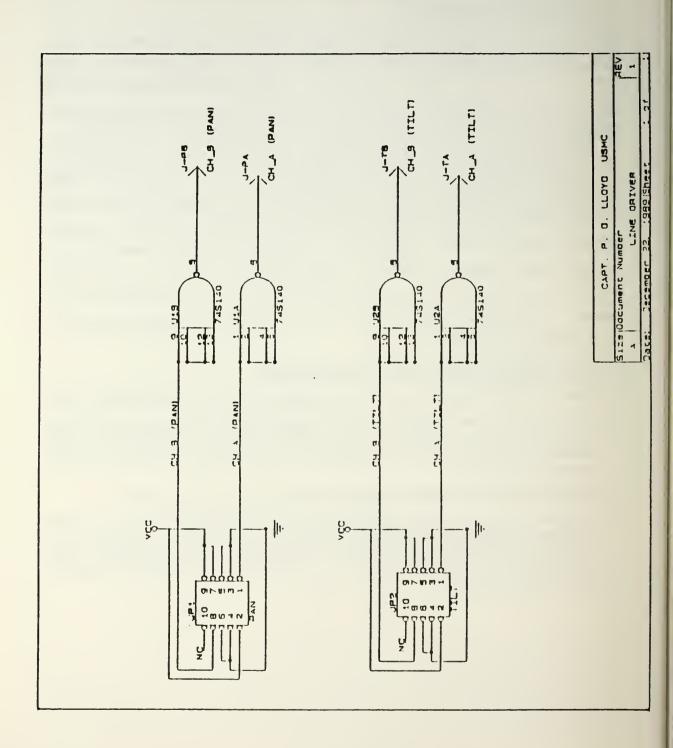
The portion of the system that will be located outdoors has been weatherproofed and is ready to be placed in service. Printed circuit board plans for the remainder of the system have been developed, but final implementation of the system is still ongoing. Once the system is fully operation additional testing should be performed in order to verify the completed system's performance. Although the laboratory results indicate that the system is capable of meeting all of the design criteria except for the required resolution on the Pan axis, the system must be further tested in a non-laboratory environment. "...The proof of a good design rests in the ability of the system to function in the outside world." [Ref 21]

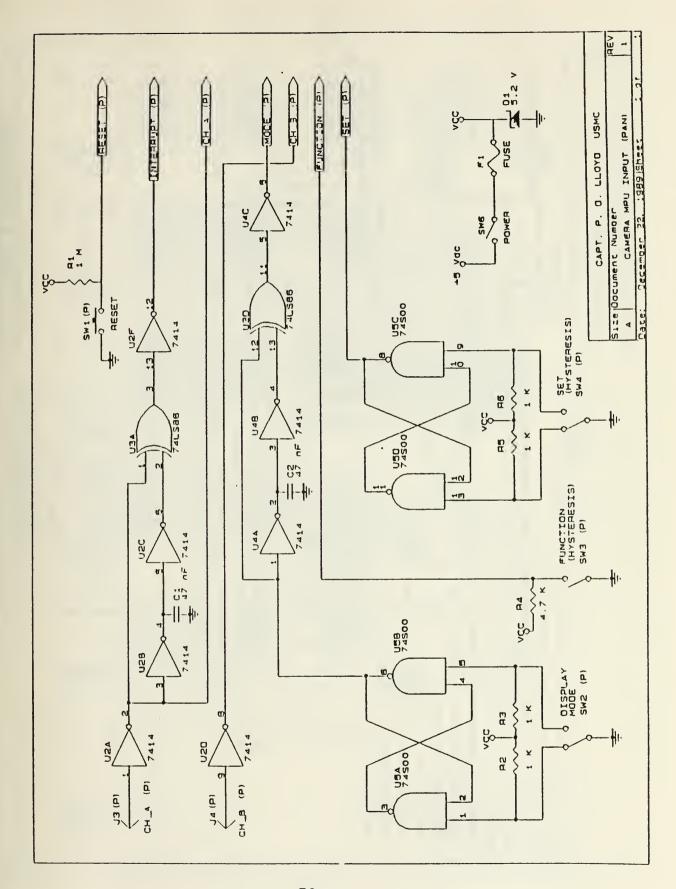
B. RECOMMENDATIONS FOR FURTHER WORK

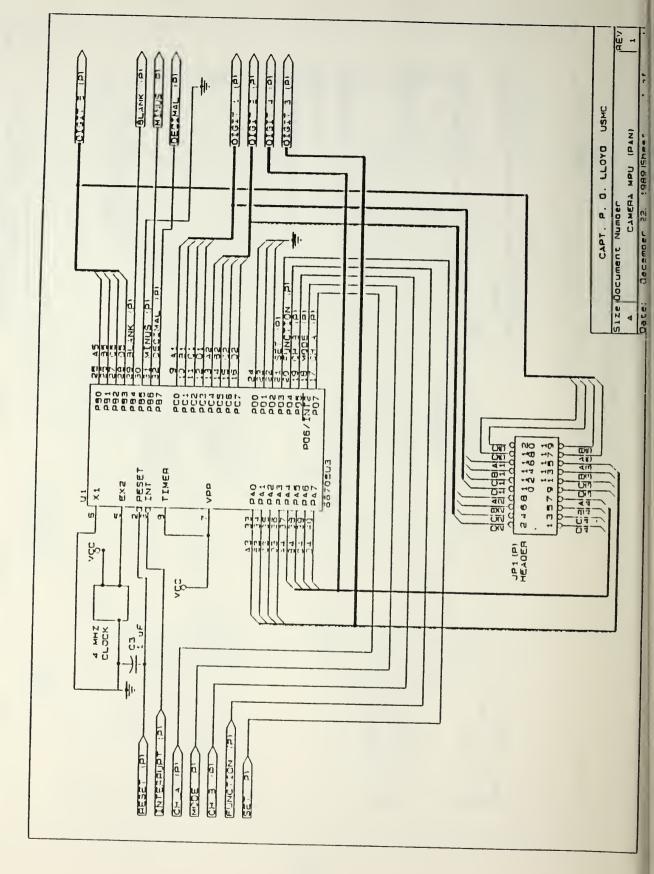
There are several areas for follow-on work with this project. Some possibilities are:

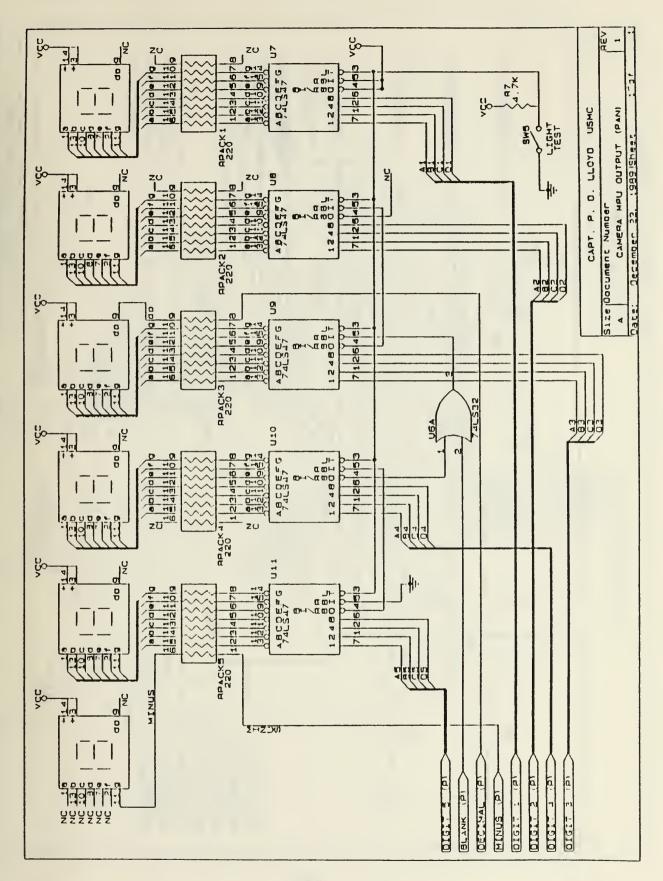
- Incorporate the measurement system's output into the video image being created by the video camera. This would permit a permanent record of the position information to be stored with the video image and would facilitate identification of the image at a later date.
- Design and build an automatic feedback control system for the camera.
- Implementation of a second video camera at the NPS, together with the NPS modified IRSTD, would permit triangulation of a target and would consequently provide range information which is not currently available. This information could provide valuable additional information to those who are developing the signal processing algorithms.

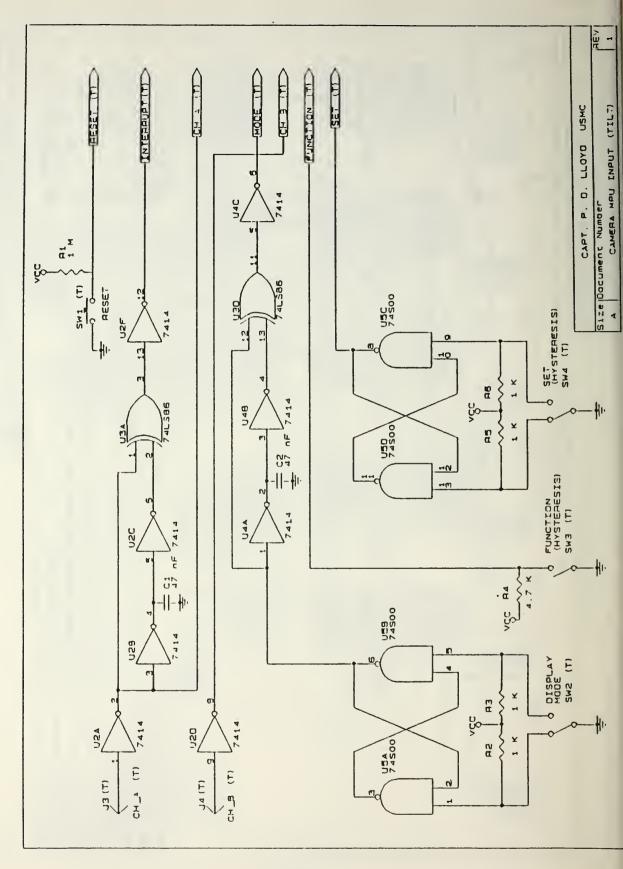
APPENDIX A. SCHEMATIC DIAGRAMS

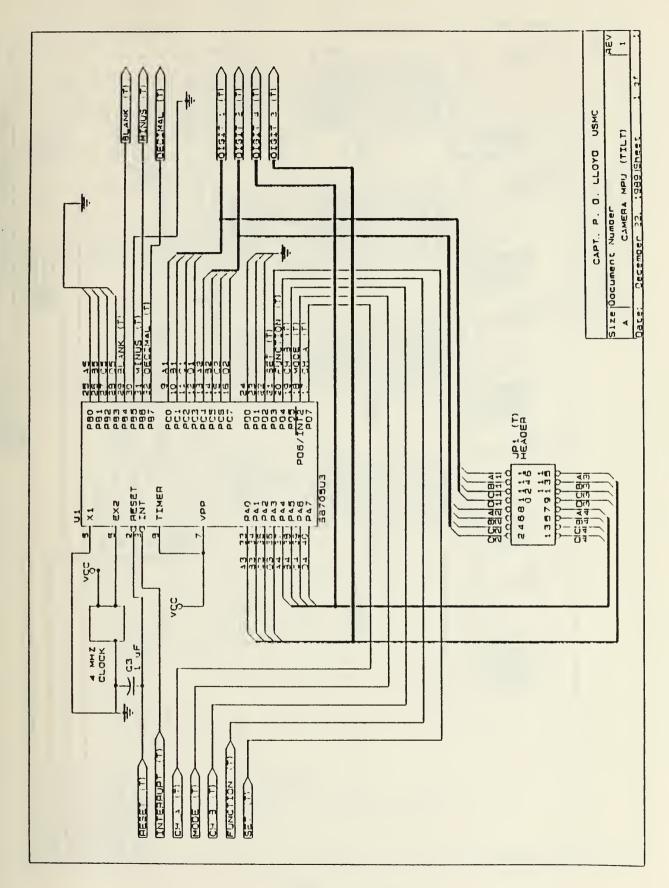


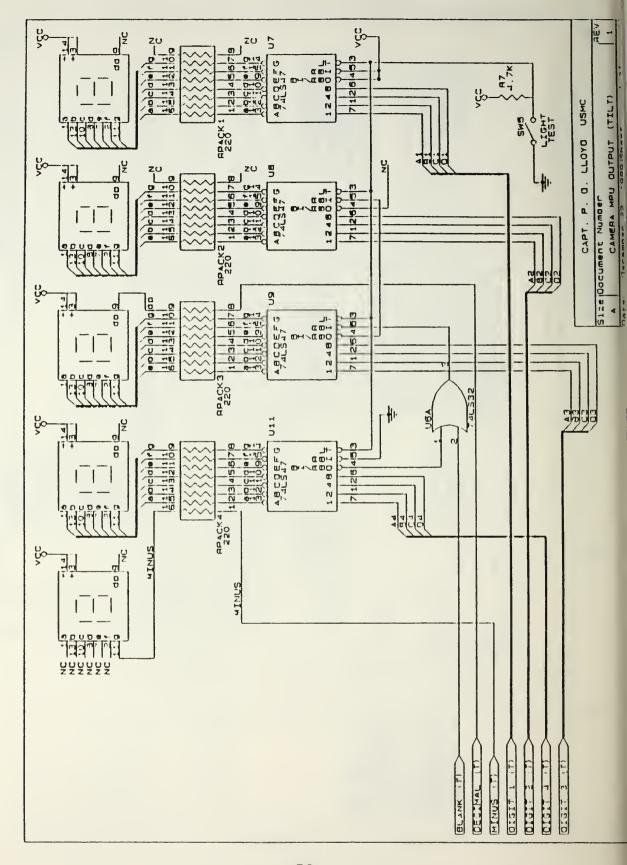


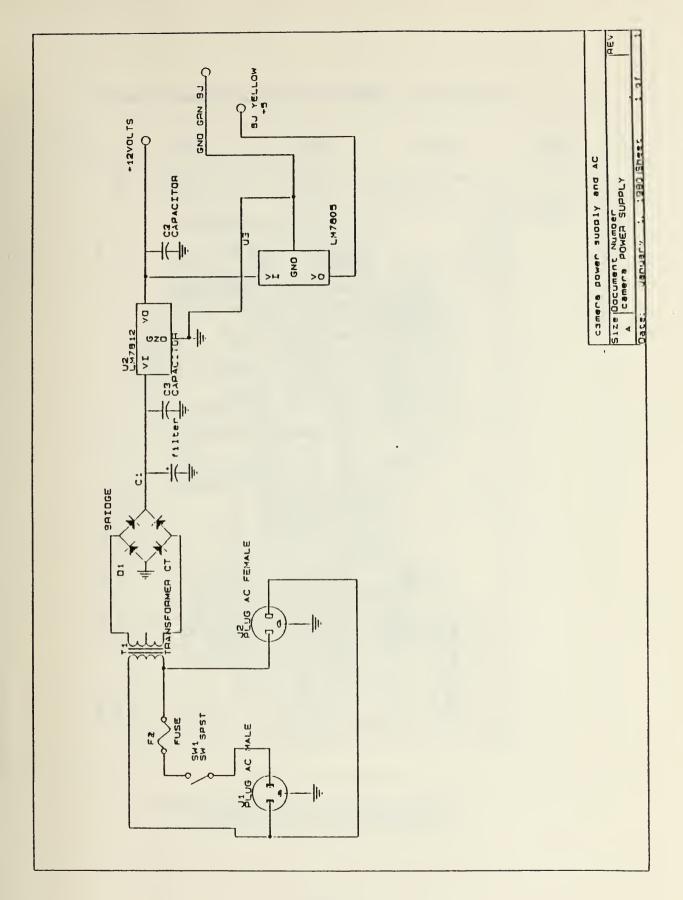




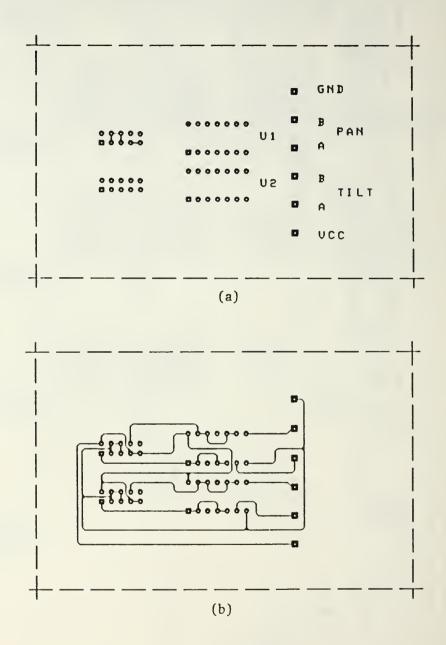




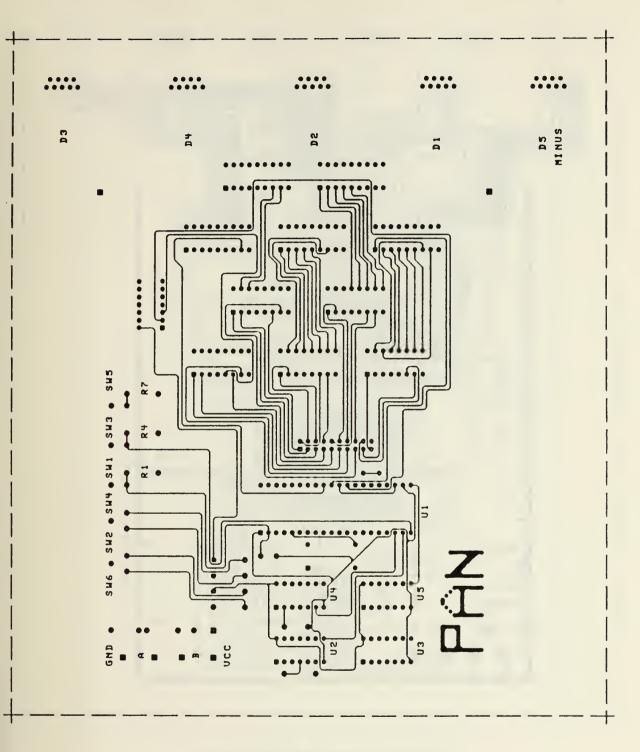




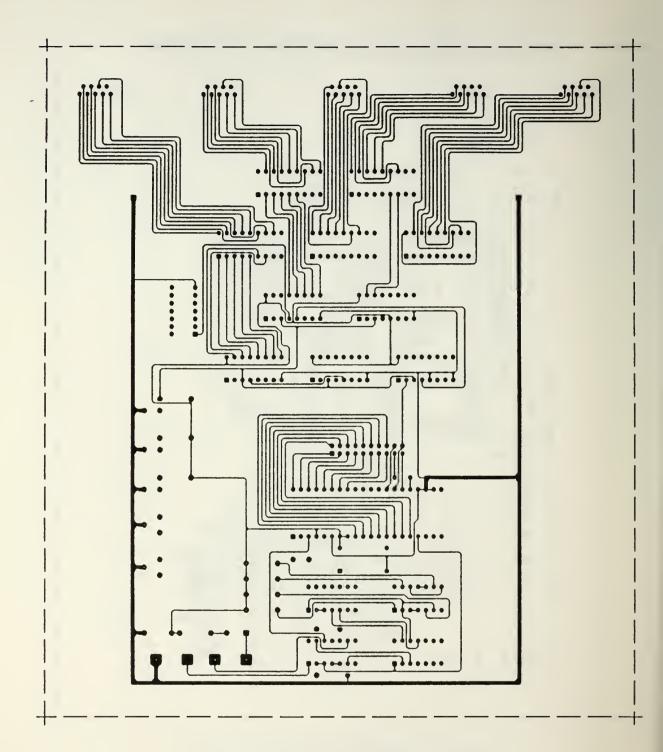
APPENDIX B. PRINTED CIRCUIT BOARD PLANS



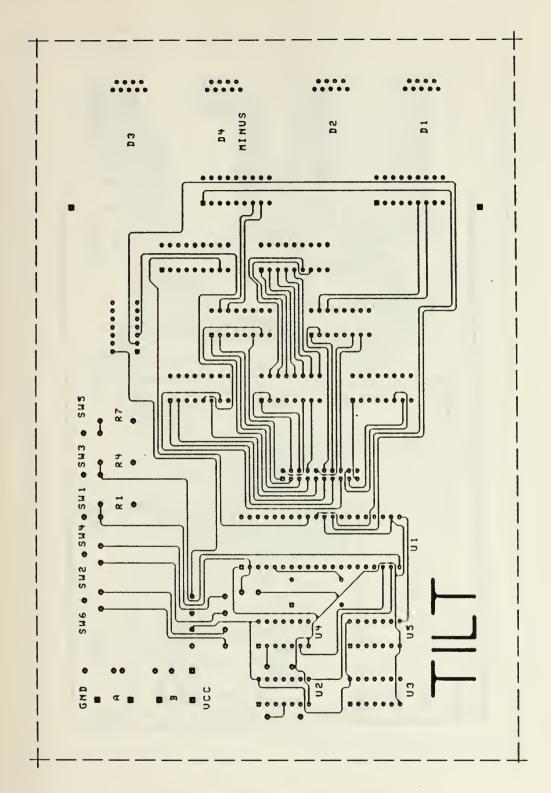
Line Driver, (a) Front and (b) Back. Full scale.



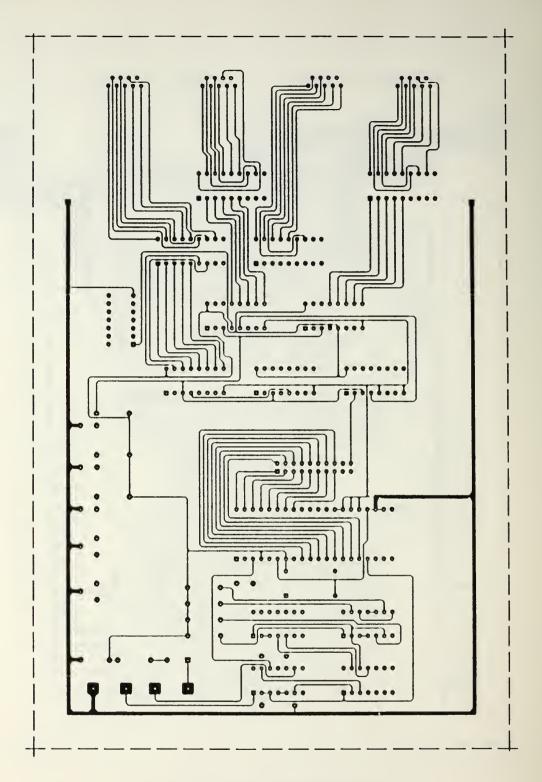
Pan MPU, Front. 90 % of full scale.



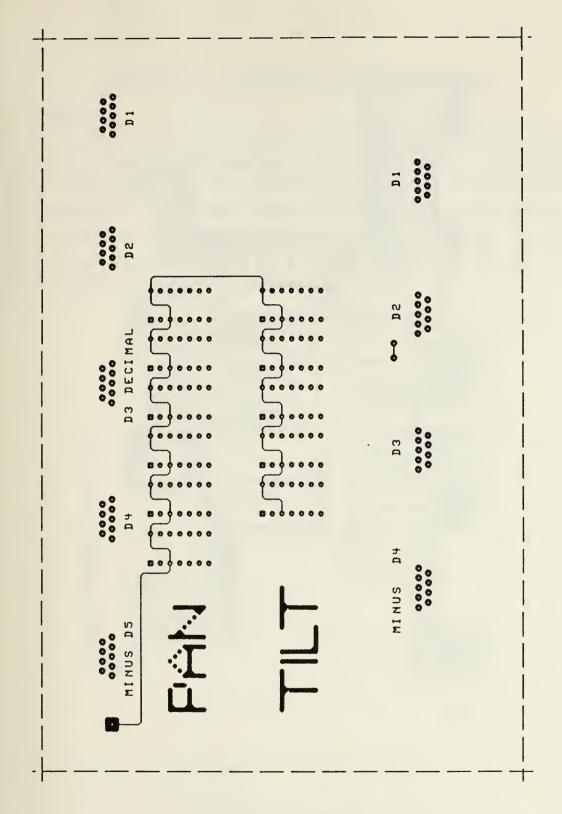
Pan MPU, Back. 90 % of full scale.



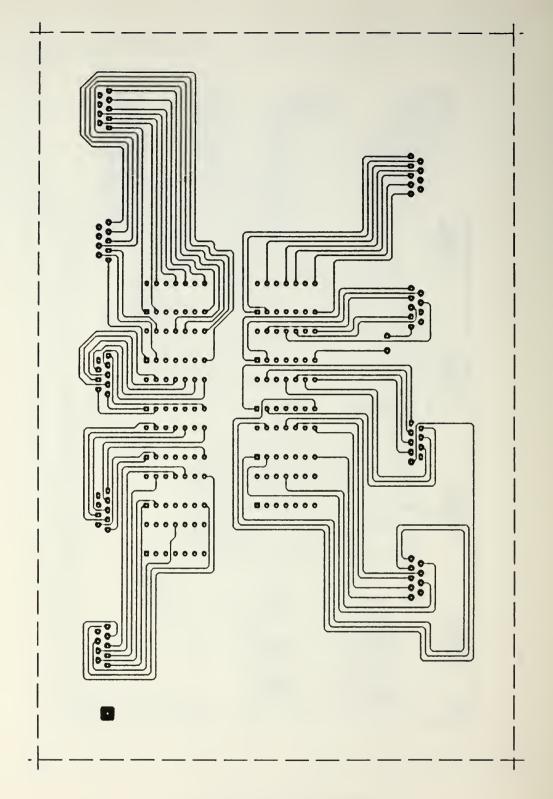
Tilt MPU, Front. 85 % of full scale.



Tilt MPU, Back. 85 % of full scale.



Display, Front. Full scale.



Display, Back. Full scale.

APPENDIX C. MICROPROCESSOR PROGRAMS

A. GENERAL

Sections B and C of this Appendix are the listing files for the two MPU programs written for the signal processor subsystems. The theory of operation of the two programs is identical and is most clearly described by Figure 31. The detailed operation of the Initialization, Mode Change, Blink, Output Display and Hysteresis Modify routines is described by the comments which accompany each of the programs. In addition to the detailed description provided by the program comments, the operation of the Count Routine is also explained in Chapter IV.

B. PAN

```
POSITION DETERMINING PROGRAM (AZIMUTH)
 1
                                         TTL
 2
                                                          LATEST REVISION
                                                                                           9 MAY 89
 3
                                 ٠
                                                           FILE NAME
                                                                                           PAN.ASM
 4
 5
                                 ** PROGRAM DESCRIPTION
 6
                                 **
 7
                                 **
 8
 9
                                 ** I/O REGISTER ADDRESSES
10
                                 **
              0000
11
                                 PORTA
                                         EQU
                                                  $0000
                                                            1/0 PORT A
12
              0001
                                 PORT8
                                         EQU
                                                  $0001
                                                            1/0 PORT B
              0002
                                                  $0002
13
                                 PORTC
                                         EQU
                                                            I/O PORT C
                                                  $0003
14
              0003
                                 PORTD
                                         EQU
                                                            INPUT PORT D
15
16
                                 ** DATA DIRECTION REGISTER OFFSET
                                 **
17
              0004
                                 DDR
18
                                         EQU
                                                  4
                                                           (eg. DDR FOR PORT A IS PORTA+DDR )
19
                                 **
                                 ** OTHERS
20
21
                                 **
22
              8000
                                 TIMER
                                         EQU
                                                  $0008
                                                           EIGHT BIT TIMER REGISTER.
23
              0009
                                 TCR
                                          EQU
                                                  $0009
                                                           TIMER CONTROL REGISTER.
              000A
                                                  $000A
24
                                         EQU
                                                           MISCELLANEOUS REGISTER.
                                 MR
25
             0010
                                         EQU
                                                  $0010
                                                           START OF ON-CHIP RAM(112 - 31 FOR STACK)
                                 RAM
             0080
                                         EQU
                                                  $0080
26
                                 ZROM
                                                           PAGE ZERO OF ROM.
27
             0100
                                 ROM
                                         EQU
                                                  $0100
                                                           START OF MAIN ROM.
28
                                 MOR
                                         EQU
                                                  $0F38
                                                           MASK OPTION REGISTER.
             0F38
29
                                        EQU
                                                  $0FF8
                                                           LOCATION OF INTERRUPT VECTORS.
             OFF8
                                 INTRPT
                                                  $1000
30
             1000
                                 MEMSIZ EQU
                                                           MEMORY ADDRESS SIZE.
                                 **
31
32
                                 ** EQUATES
                                 **
33
34
             0001
                                 BITO
                                         EQU
                                                  1
35
             0002
                                 BIT1
                                         EQU
                                                  2
             0004
36
                                 BIT2
                                         EQU
                                                  4
37
             0008
                                 BIT3
                                         EQU
                                                  8
38
             0010
                                 BIT4
                                         EQU
                                                  16
39
             0020
                                         EQU
                                                  32
                                 BIT5
40
             0040
                                 BIT6
                                         EQU
                                                  64
             0800
                                                  128
41
                                BIT7
                                         EQU
                                 **
42
43
             0000
                                во
                                         EQU
                                                  0
44
             0001
                                         EQU
                                B1
                                                  1
45
             0002
                                         EQU
                                                  2
                                B2
             0003
46
                                B3
                                         EQU
                                                  3
47
             0004
                                         EQU
                                                  4
                                B4
48
             0005
                                B5
                                         EQU
                                                  5
49
             0006
                                B6
                                         EQU
                                                  6
50
             0007
                                в7
                                         EQU
                                                  7
51
                                **
52
                                 ** EQUATES FOR THE TIMER CONTROL REGISTER
53
                                ***
54
55
             0007
                                TIR
                                         EQU
                                                  7
                                                           TIMER INTERRUPT REQUEST. 1 = REQUEST, 0 = NO REQ.
                                                           TIMER INTERRUPT MASK. 1 = DISABLED, 0 = ENABLED.
EXTERNAL OR INTERNAL CLOCK SOURCE. 1 = EXT, 0 = INT
56
             0006
                                TIM
                                         EQU
                                                  6
57
             0005
                                TIN
                                         EQU
                                                  5
58
             0004
                                         EQU
                                                  4
                                                           EXTERNAL CLOCK ENABLE. NOT USED.
                                TEE
59
             0003
                                         EQU
                                                  3
                                                           PRESCALER CLEAR. NOT USED.
                                PSC
60
             0002
                                PS2
                                         EQU
                                                  2
                                                           (PS2) --
             0001
61
                                PS1
                                         EQU
                                                           (PS1)
                                                                     |-- PRESCALER SELECT BITS.
```

62 63	0000	PS0	EQU	0	(PSO) -	-				
64			TES FOR	THE STATE	US BYTE,	'STAT'.				
65		***								
66		***								
67		**	5011	-		DECTIONS	4 110	0 - 00	16.1	
68 69	0007 0006	MOD 32	EQU		COUNT DI					
70	0005	FLASH	EQU	5			Y? 1 = Y			
71	0004	POSCT	EQU	4	DISPLAY	POSITION	OR COUNT	? 1 = 1	POS, 0 =	COUNT.
72	0003	L_SET	EQU	3	VALUE OF				·	
73	0002	NEGTIV	EQU	2	IS 'BCDC		VE NUMBER	? 1 = 1	YES, $0 =$	NO.
74		***		1	NOT USED	-				
75		***		0	NOT USED	•				
76 77		***								
78			FOLIATES	AND DESC	RIPTIONS.					
79		***		,,,,,						
80		***								
81		***	PORT A	(1/0)						
82		***								
83 84		***	+	*	DIGIT #4	+	++ 	BCD DI	+ CIT #7	1
85		***	+	-+		+	 ++			
86		***	I D4				D3			A3
87		***	+	-+	-+	+	+			
88		*** BIT	7	6	5	4	3	2	1	0
89		***								
90		***	2007.0	47.40						
91 92		***	POKIB	(1/0)						
93		***	+	-+	-+	+	+		+	
94		***	1	DISPLA	Y CONTROL		BCD DIGI	T #5 (MC	OST SIGN	[FICANT)
95		***		-+	-+	+	÷+		+	·
96		***	DECPT	POSTI	٧	BLANK	D5	C5	B5	A5
97		*** BIT	+	-+	-+	+	+		+	
98 99		***	7	6	5	4	3	2	1	0
100	0007	DECPT	EQU	7	TO DISPL	AY THE D	ECIMAL PO	INTDI	ECPT IS	CLEARED
101	0006	POSTIV	EQU	6			NEGATIVE			
102		***			MINUS SI	GN.				
103	0004	BLANK	EQU	4			2 AND 3			
104 105		***					RE ALWAYS		D.	
106		***			ו ווטוע	15 MEVEK	BLANKED.			
107		***	PORT C	(1/0)						
108		***		(-, -,						
109		***	+	-+	-+	•			•	·
110		***		BCD	DIGIT #2		BCD DIGI	T #1(LE	AST SIGN	FICANT)
111 112		***	1 03	-+	-+	+	++ 01	C1	+ l p1	1 41 1
113		***	D2	C2	BZ	A2	D1		B1	A1
114		*** BIT	7	. 6	. 5	4	3	2	1	0
115		***								
116		***								
117		***	PORT D	(INPUT	ONLY)					
118 119		***	4	-4	-+					
120		***			CH_B				l	
121		***	+	-+	-+	+	JE1		 	 +
122		*** BIT	7	6	5	4	3	2	1	0
123		***								
124	0007	CH_A	EQU		INDICATE					
125	0006	INT2	EQU	6			SED TO CH			DES.
126 127	0005 0004	CH_B FUNCT	EQU	5			ATUS OF C			III ALLON
127	0004	FUNCT	EWU	4	OSED 10	PUI THE	PKUGKAM I	N A MUDI	E IHAI W	ILL ALLOW

128			***			'HYST' TO BE INCREMENTED.
129		0003		Q U	3	INCREMENTS 'HYST' WHEN TOGGLED AND FUNCT IS LOW.
130			***			
131			***			*******************
132			***			
133			**			DAM WARTARIES
134			**			RAM VARIABLES *
135			**			-
136			**			
137			** 050501	/F MEMOR		FOR THE DROCDAM MARIADIES
138 139			** KESEK	/E MEMUR	KT SPACE I	FOR THE PROGRAM VARIABLES.
140	0000			ATA		
141	0000		**	7010		
142			**			
143	0000			ARSOLUTE	(ABSOLU	TE ADDRESSING USED HERE TO RELATIVE DIRECTIVE)
144	••••		**			
145	0010		(ORG	RAM	START OF RAM.
146			**			
147			*** BINA	RY COUNT	Γ.	
148	0010		BINCT F	RMB	3	
149		0010	HIBIN E	QU	BINCT	HI BYTE.
150		0011	MIDBIN E	QU	BINCT+1	MIDDLE BYTE.
151		0012	LOBIN E	QU	BINCT+2	LO BYTE.
152			**			
153			*** POSI1	TION POI	INTERS.	
154	0013			RMB	4	EACH BYTE POINTS TO A POSITION IN THE
155			**			TABLE THAT CONTAINS ONE OR TWO DIGITS
156			**			OF THE BCD POSITION.
157		0013		QU	PTR	MOST SIGNIFICANT DIGITS.
158		0014		QU	PTR+1	
159		0015		OU.	PTR+2	LEACT CICHIFICANT DICIT
160 161		0016	PTR1 6	QU	PTR+3	LEAST SIGNIFICANT DIGIT.
162			*** COUNT	T DOTATE	- 00	
163	0017			RMB	3	EACH BYTE POINTS TO A POSITION IN THE
164	0017		**	Ano	,	TABLE THAT CONTAINS TWO OF THE DIGITS
165			**			IN THE BCD COUNT.
166		0017	CTPTR3 E	OU	CTPTR	MOST SIGNIFICANT DIGITS.
167		0018	CTPTR2		CTPTR+1	
168		0019		QU		LEAST SIGNIFICANT DIGITS.
169			**			
170			*** BCD F	POSITION	IN DEGRI	EES.
171	001A		DEGRES F	RMB	4	
172		001A	HUNDEG 8	QU	DEGRES	CONTENTS X 100.000
173		001B	ONEDEG E	QU	DEGRES+1	CONTENTS X 1.000
174		001C	HUNDTH 6	QU	DEGRES+2	CONTENTS X 0.010
175		001D	THOUTH E	QU	DEGRES+3	+ CONTENTS X 0.001
176			***			•••••
177			***			POSITION IN DEGREES
178			**			
179			*** BCD (_	
180	001E	0045			3	00HTEHTO V 40 000
181		001E	TENTHO E			CONTENTS X 10,000
182		001F	HUNDRD E TENONE E	-00	BCDCT+1	
183 184		0020	TENUNE E	:40	BCDCT+2	+ CONTENTS X 1
185			***			NUMBER OF PULSES COUNTED
186			***			NUMBER OF PUESES COUNTED
187				PECIC O	CHINTER	POINTS TO A NUMBER IN THE TABLE THAT IS THE
188			***			RESIS PRESENT IN THE SYSTEM. INITIALIZED TO 7.
189	0021		HYSTPT F		1	need and an ine didition and interest 10 /
190	0021		**		•	
191			*** POST	TION INC	CREMENT.	CONTAINS A NUMBER, THAT WHEN MULTIPLIED BY 0.00
192			***			F DEGREES THAT THE POSITION COUNTER (BCDPOS) IS
193			***			ED OR DECREMENTED DURING PROGRAM EXECUTION.
-						

			***	THE 144		POOLING! DETERMINED EVOCATHENTALLY CHOILD DE
194			***	THE VA	LUE UF	POSINC', DETERMINED EXPERIMENTALLY, SHOULD BE THE PROGRAM IS DESIGNED WORK WITH INTEGERS ONLY
195			***	7.0312	. SINCE	ROUNDED TO 7. TO REDUCE THE CUMULATIVE EFFECT OF
196			***			
197			***			EVERY 32 COUNTS 'POSINC' IS SET EQUAL TO 8. THIS SOME CUMULATIVE ERROR THAT IS ACCOUNTED FOR BY
198			***			IC' TO 7 INSTEAD OF 8 WHEN THE COUNT REACHES A
199			***			The state of the s
200			***	VALUE	UF 16384	(2^14).
201						
202	0022		POSINC	RMB	1	
203						LIGHT TO SUBMITTE THE SESSON OF PARVIACU ON
204						S. USED TO ELIMINATE THE EFFECTS OF BACKLASH ON
205			***	THE PO	SITION M	EASUREMENTS.
206						THE THRESHIP WALLS ACTION THE
207	0023		HYST	RMB	1	THE THRESHOLD VALUE DETERMINED
208	000/					EXPERIMENTALLY.
209	0024		HYSTCT	RMB	1	CURRENT AMOUNT OF HYSTERESIS MEASURED.
210						TO WEED TRACK OF INIT TO COINC ON
211			***	IIUS BYTE	. USED	TO KEEP TRACK OF WHAT IS GOING ON.
212						AMBROUT ATATUA
213	0025		STAT	RMB	1	CURRENT STATUS.
214	0026		LSTAT	RMB	1	PREVIOUS/LAST STATUS. USED TO KEEP TRACK OF
215			***			L_SET ONLY.
216						
217			***			D IN CONJUNCTION WITH THE TIMER PRESCALER AND THE
218						ACK OF ONE SEC. INTERVALS. USED IN BLINKING THE
219			***			TALLY SET TO 31, WHEN THE 'FLASH' BIT OF 'STAT'
220			***			IS DECREMENTED EACH CLOCK INTERRUPT (APPROX. 31
221			***			. RESET TO 31 WHEN CONTENTS GO TO ZERO.
222			***	WHEN (TIMCT)=0	THE DISPLAY WILL TOGGLE.
223			***			
224	0027		TIMCT	RMB	1	
225			**			
226				ENDS		
222			**			
227						•
228			***			•
228 229			***	*****	****	************
228 229 230			**	*****	*****	*
228 229 230 231			***	*****	*****	PAGE ZERO ROM
228 229 230 231 232			**			PAGE ZERO ROM *
228 229 230 231 232 233			** ** ** **			*
228 229 230 231 232 233 234			** ** ** ** ** ** **		*****	PAGE ZERO ROM
228 229 230 231 232 233 234 235			** ** ** ** ** **		*****	PAGE ZERO ROM *
228 229 230 231 232 233 234 235 236			** ** ** ** ** ** **		*****	PAGE ZERO ROM
228 229 230 231 232 233 234 235 236 237			** ** ** ** ** **	*****	*****	PAGE ZERO ROM
228 229 230 231 232 233 234 235 236 237 238	0000		**		*****	PAGE ZERO ROM
228 229 230 231 232 233 234 235 236 237 238 239			** ** ** ** ** ** **	CODE	·******	PAGE ZERO ROM ***********************************
228 229 230 231 232 233 234 235 236 237 238 239 240	0000		** ** ** ** ** ** ** **	*****	*****	PAGE ZERO ROM
228 229 230 231 232 233 234 235 236 237 238 239 240 241	0080		**	CODE ORG	I ZROM	PAGE ZERO ROM ***********************************
228 229 230 231 232 233 234 235 236 237 238 239 240 241 242			** ** ** ** ** ** ** **	CODE	I ZROM	PAGE ZERO ROM ***********************************
228 229 230 231 232 233 234 235 236 237 238 239 240 241 242 243	0080		** ** ** ** ** ** ** **	CODE ORG	I ZROM	PAGE ZERO ROM ***********************************
228 229 230 231 232 233 234 235 236 237 238 239 240 241 242 243 244	0080	0080	** ** ** ** ** ** ** ** RESTRT	CODE ORG RELATIV	I ZROM	PAGE ZERO ROM ***********************************
228 229 230 231 232 233 234 235 236 237 238 239 240 241 242 243 244 245	0080	0080	** ** ** ** ** ** ** ** RESTRT ***	CODE ORG RELATIV	I ZROM /E	PAGE ZERO ROM ***********************************
228 229 230 231 232 233 234 235 236 237 238 239 240 241 242 243 244 245 246	0080	0080	** ** ** ** ** ** ** ** RESTRT	CODE ORG RELATIV	I ZROM /E	PAGE ZERO ROM ** ** ** ** ** ** ** ** **
228 229 230 231 232 233 234 235 236 237 238 239 240 241 242 243 244 245 246 247	0080	0080	** ** ** ** ** ** ** ** RESTRT ***	CODE ORG RELATIV	I ZROM /E	PAGE ZERO ROM ***********************************
228 229 230 231 232 233 234 235 236 237 238 239 240 241 242 243 244 245 246 247 248	0080	0080	** ** ** ** ** ** ** RESTRT ** ** ** ** ** ** ** ** **	CODE ORG RELATIV	I ZROM /E	PAGE ZERO ROM ** ** ** ** ** ** ** ** **
228 229 230 231 232 233 234 235 236 237 238 239 240 241 242 243 244 245 246 247 248 249	0080	0080	** ** ** ** ** ** ** ** RESTRT ** ** ** ** ** ** ** ** **	CODE ORG RELATIV	I ZROM /E \$	PAGE ZERO ROM ** ** ** ** ** ** ** ** **
228 229 230 231 232 233 234 235 236 237 238 239 240 241 242 243 244 245 246 247 248 249 250	0080	0080	** ** ** ** ** ** ** RESTRT ** ** ** ** ** ** ** ** **	CODE ORG RELATIV	I ZROM /E \$	PAGE ZERO ROM ** ** ** ** ** ** ** ** **
228 229 230 231 232 233 234 235 236 237 238 239 240 241 242 243 244 245 246 247 248 249 250 251	0080	0080	** ** ** ** ** ** ** ** RESTRT ** ** ** ** ** ** ** ** **	CODE ORG RELATIV	I ZROM /E \$	PAGE ZERO ROM ** ** ** ** ** ** ** ** **
228 229 230 231 232 233 234 235 236 237 238 239 240 241 242 243 244 245 246 247 248 249 250	0080	98	** ** ** ** ** ** ** ** ** **	CODE ORG RELATIV	I ZROM /E \$	PAGE ZERO ROM ** ** ** ** ** ** ** ** **
228 229 230 231 232 233 234 235 236 237 238 239 240 241 242 243 244 245 246 247 248 249 250 251	0080		** ** ** ** ** ** ** ** ** **	CODE ORG RELATIV EQU	I ZROM /E \$	PAGE ZERO ROM ** NITIALIZATION ROUTINE. PAGE ZERO ROM. RELATIVE ADDRESSING MUST BE USED FOR THE BRANCH. THIS IS THE ENTRY POINT WHEN THE RESET SWITCH IS PUSHED.
228 229 230 231 232 233 234 235 236 237 238 239 240 241 242 243 244 245 246 247 248 249 250 251 252 253 254	0080 0080 0080	98	** ** ** ** ** ** ** ** ** **	CODE ORG RELATIV	I ZROM /E \$	PAGE ZERO ROM ** NITIALIZATION ROUTINE. PAGE ZERO ROM. RELATIVE ADDRESSING MUST BE USED FOR THE BRANCH. THIS IS THE ENTRY POINT WHEN THE RESET SWITCH IS PUSHED. ** ** ** ** ** ** ** ** ** ** ** ** *
228 229 230 231 232 233 234 235 236 237 238 239 240 241 242 243 244 245 246 247 248 249 250 251 252 253	0080 0080 0080	98	** ** ** ** ** ** ** ** ** **	CODE ORG RELATIV	I ZROM /E \$	PAGE ZERO ROM ** ** ** ** ** ** ** ** **
228 229 230 231 232 233 234 235 236 237 238 239 240 241 242 243 244 245 246 247 248 249 250 251 252 253 254	0080 0080 0080 0080 0081	98 90	** ** ** ** ** ** ** ** ** **	CODE ORG RELATIVE	ZROM /E \$ INITIA	PAGE ZERO ROM ** ** ** ** ** ** ** ** **
228 229 230 231 232 233 234 235 236 237 238 239 240 241 242 243 244 245 246 247 248 249 250 251 252 253 254 255	0080 0080 0080 0080 0081	98 90 AE 10	** ** ** ** ** ** ** ** ** **	CODE ORG RELATIVE EQU SEI RSP LDX	ZROM /E \$ INITIA	PAGE ZERO ROM ** ** ** ** ** ** ** ** **
228 229 230 231 232 233 234 235 236 237 238 239 240 241 242 243 244 245 246 247 248 249 250 251 252 253 254 255 256	0080 0080 0080 0080 0081 0082 0084	9B 9C AE 10 7F	** ** ** ** ** ** ** ** ** **	CODE ORG RELATIVE EQU SEI RSP LDX CLR	ZROM /E \$ INITIA	PAGE ZERO ROM ** ** ** ** ** ** ** ** **
228 229 230 231 232 233 234 235 236 237 238 239 240 241 242 243 244 245 246 247 248 249 250 251 252 253 254 255 256 257	0080 0080 0080 0081 0082 0084 0085	98 9C AE 10 7F 5C	** ** ** ** ** ** ** ** ** **	CODE ORG RELATIVE EQU SEI RSP LDX CLR INCX	ZROM /E \$ INITIA	PAGE ZERO ROM ** ** ** ** ** ** ** ** **

260			*** DIRECTION FROM THE MOST CCW POSITION
2 61			*** AFTER A RESET.
2 62			***
263	A800		ABSOLUTE BACK TO ABSOLUTE ADDRESSING.
264			***
265			*******************************
266			***
			*** ESTABLISH I/O PORTS.
267			ttt
268			
269	008A	A6 FF	LDA #-1 PORTS A,B,C ARE CONFIGURED AS
270	008C	B7 04	STA PORTA+DDR ALL OUTPUT. PORT D IS ALL INPUT
271	008E	B7 05	STA PORTB+DDR SO THERE IS NO MASK TO SET.
272	0090	B7 06	STA PORTC+DDR
273			***
274			***
275	0092	CD 03 4E	JSR OUTCT COUNT IS TO BE DISPLAYED INITIALLY.
276	***		***
277			***************************************
			*** SET UP THE STATUS REGISTER.
278			***
279			
280	0095	A6 08	LDA #%00001000
281	0097	B4 03	AND PORTD > SET UP 'L_SET' BIT OF 'STAT'.
282	0099	B7 25	STA STAT
283			***
284	009B	1C 25	BSET MOD 32,STAT 0 IS MODULO 32.
285			**
286			***************************************
287			***
			*** INITIALIZE HYCTCT
288			INTITACIZE MISICI.
289			***
290	0090	A6 08	LDA #08
291	009F	B7 23	STA HYST
292	00A1	B7 21	STA HYSTPT
293			***

294			*********************
294 295			**
294 295 296			**
294 295 296 297			** ** SET UP THE TIMER FOR A 4 MHZ CRYSTAL / 4 = 1 MHZ CLOCK. ***
294 295 296 297 298			** ** SET UP THE TIMER FOR A 4 MHZ CRYSTAL / 4 = 1 MHZ CLOCK. *** *** NOTE: THE MASK OPTION REGISTER IS IN ROM. IT IS SET UP AT
294 295 296 297 298 299			** ** SET UP THE TIMER FOR A 4 MHZ CRYSTAL / 4 = 1 MHZ CLOCK. *** *** NOTE: THE MASK OPTION REGISTER IS IN ROM. IT IS SET UP AT THE END OF THE PROGRAM.
294 295 296 297 298 299 300			** ** SET UP THE TIMER FOR A 4 MHZ CRYSTAL / 4 = 1 MHZ CLOCK. *** *** NOTE: THE MASK OPTION REGISTER IS IN ROM. IT IS SET UP AT *** THE END OF THE PROGRAM.
294 295 296 297 298 299 300 301			** ** ** SET UP THE TIMER FOR A 4 MHZ CRYSTAL / 4 = 1 MHZ CLOCK. *** *** NOTE: THE MASK OPTION REGISTER IS IN ROM. IT IS SET UP AT *** THE END OF THE PROGRAM. *** *** *** *** *** *** ***
294 295 296 297 298 299 300 301 302			** ** ** ** ** ** ** ** *** *** *** *** * **
294 295 296 297 298 299 300 301	00A3	A6 47	** ** ** SET UP THE TIMER FOR A 4 MHZ CRYSTAL / 4 = 1 MHZ CLOCK. *** *** NOTE: THE MASK OPTION REGISTER IS IN ROM. IT IS SET UP AT *** THE END OF THE PROGRAM. *** *** *** *** *** *** ***
294 295 296 297 298 299 300 301 302	00A3	A6 47	** ** ** ** ** ** ** ** *** *** *** *** * **
294 295 296 297 298 299 300 301 302 303	00A3	A6 47	** ** ** ** ** ** ** ** *** *** *** *** **
294 295 296 297 298 299 300 301 302 303 304	00A3	A6 47	** ** ** ** ** ** ** ** *** *** *** *** *** *** *** *** *** *** *** *** ** *** *** *** *** *** *** *** *** *** *** *** *** ** *** *** *** *** *** *** *** *** *** *** *** *** ** *** *** *** *** *** *** *** *** *** *** *** *** ** *** *** *** *** *** *** *** *** *** *** *** *** ** *** *** *** *** *** *** *** *** *** *** *** *** **
294 295 296 297 298 299 300 301 302 303 304 305 306			** ** ** ** ** ** ** ** ** **
294 295 296 297 298 299 300 301 302 303 304 305 306 307	00A3	A6 47 B7 09	** ** ** ** ** ** ** ** ** **
294 295 296 297 298 299 300 301 302 303 304 305 306 307 308			** ** ** ** ** ** ** ** ** **
294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309			** ** ** ** ** ** ** ** ** **
294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309 310			** ** ** ** ** ** ** ** *** *** *** *** *** *
294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309 310 311	00A5	B7 09	** ** ** ** ** ** ** ** ** **
294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309 310		B7 09	** ** ** ** ** ** ** ** *** *** *** *** *** *
294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309 310 311	00A5	B7 09	** ** ** ** ** ** ** ** ** **
294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309 310 311 312	00A5	B7 09	** ** ** ** ** ** ** ** ** **
294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309 310 311 312 313	00A5	B7 09	** ** ** ** ** ** ** ** ** **
294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309 311 312 313 314 315	00A5	B7 09	** ** ** ** ** ** ** ** ** **
294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309 310 311 312 313 314 315 316	00A5 00A7 00A9	B7 09 A6 FF B7 08	** ** ** ** ** ** ** ** ** **
294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309 310 311 312 313 314 315 316 317	00A5 00A7 00A9	B7 09 A6 FF B7 08	** ** ** ** ** ** ** ** ** **
294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309 310 311 312 313 314 315 316 317 318	00A5 00A7 00A9	B7 09 A6 FF B7 08	** ** ** ** ** ** ** ** ** **
294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309 310 311 312 313 314 315 316 317 318 319	00A5 00A7 00A9	B7 09 A6 FF B7 08	** ** ** ** ** ** ** ** ** **
294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309 310 311 312 313 314 315 316 317 318 319 320	00A5 00A7 00A9	B7 09 A6 FF B7 08	** ** ** ** ** ** ** ** *** *** *** *** *** *** *** *** *** *** *** *** ** *** *** *** *** *** *** *** *** *** *** *** *** ** *** *** *** *** *** *** *** *** *** *** *** *** ** *** *** *** *** *** *** *** *** *** *** *** *** ** *** *** *** *** *** *** *** *** *** *** *** *** ** *** *** *** *** *** *** *** *** *** *** *** *** **
294 295 296 297 298 299 300 301 302 303 304 305 306 307 310 311 312 313 314 315 316 317 318 319 320 321	00A5 00A7 00A9	B7 09 A6 FF B7 08	** ** ** ** ** ** ** ** ** **
294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309 310 311 312 313 314 315 316 317 318 319 320 321 322	00A5 00A7 00A9	B7 09 A6 FF B7 08	** ** ** ** ** ** ** ** ** **
294 295 296 297 298 299 300 301 302 303 304 305 306 307 310 311 312 313 314 315 316 317 318 319 320 321	00A5 00A7 00A9	B7 09 A6 FF B7 08	** ** ** ** ** ** ** ** ** **
294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309 310 311 312 313 314 315 316 317 318 319 320 321 322	00A5 00A7 00A9	B7 09 A6 FF B7 08	** ** ** ** ** ** ** ** ** **
294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 310 311 312 313 314 315 316 317 318 319 320 321 322 323	00A5 00A7 00A9	B7 09 A6 FF B7 08	** ** ** ** ** ** ** ** ** **

```
326
                               **
327
      00B1
                                                       CLEAR THE INTERRUPT MASK TO GET STARTED.
328
             9A
                                       CLI
329
330
      00B2
                                       RELATIVE
                                                       RELATIVE ADDRESSING MUST BE USED FOR THE
331
                               ***
                                                       REMAINDER OF THE PROGRAM.
                               ***
332
                               *************************
333
334
335
                               ** WAIT LOOP. EXECUTES, UNTIL AN INTERRUPT OCCURS.
336
337
      00<sub>B</sub>2
             09 03 0B
                               PAUSE
                                      BRCLR
                                               FUNCT, PORTD, CHHYST WANT TO CHANGE HYST?
                                                                 YES...GO TO CHHYST.
338
339
      00B5
             06 03 04
                                       BRSET
                                               SET, PORTD, SBIT
                                                                 NO... 'SET, PORTD' SET?
      00B8
             17 25
340
                                       BCLR
                                               L_SET,STAT
                                                                      NO...CLEAR 'L_SET, STAT'
341
      OOBA
             20 F6
                                       BRA
                                               PAUSE
                                                                      AND LOOP.
342
      OOBC
             16 25
                                       BSET
                               SBIT
                                               L SET, STAT
                                                                      YES ... SET 'L SET, STAT'
343
      OOBE
             20 F2
                                       BRA
                                               PAUSE
                                                                      AND...LOOP
344
                               345
346
                               **
347
                               ** HYSTERESIS MODIFICATION ROUTINE. PERMITS MODIFICATION OF THE
348
                               ** HYSTERESIS BUFFER WITHOUT REPROGRAMMING.
340
                              **
350
      0000
             A6 40
                              CHHYST
                                      LDA
                                               #BIT6
                                                                  DISABLE TIMER INTERRUPT.
351
      00C2
             B7 09
                                               TCR
                                       STA
352
353
      00C4
             A6 08
                                               #%00001000
                                       LDA
                                                                  SAVE 'L SET'
      0006
             B4 25
354
                                      AND
                                               STAT
                                                                  INTO
355
      0008
             B7 26
                                       STA
                                               LSTAT
                                                                  'LSTAT'.
      00CA
356
             A6 08
                                       LDA
                                               #%00001000
      0000
             B4 03
357
                                      AND
                                               PORTD
                                                                  'SET, PORTD' --> ACCUMULATOR
358
      OOCE
             B1 26
                                       CMP
                                               LSTAT
                                                                  HAS THE SET SWITCH BEEN CHANGED?
359
      0000
             27 15
                                      BEQ
                                               DISPLA
360
                                                                  YES...
361
      0002
             A6 08
                                      LDA
                                               #%00001000
362
      0004
             B8 25
                                      EOR
                                               STAT
                                                                   |-->CHANGE 'L_SET, STAT',
363
      0006
             B7 25
                                      STA
                                               STAT
364
      8000
             3C 23
                                      INC
                                               HYST
                                                                  THEN INCREMENT THE HYSTERESIS
365
      00DA
             3C 21
                                      INC
                                               HYSTPT
                                                                  POINTER AND 'HYST' ...
366
                              ***
367
      OODC
             B6 21
                                      LDA
                                               HYSTPT
368
      OODE
             A1 19
                                      CMP
                                               #25
369
      00E0
             23 05
                                      BLS
                                               DISPLA
370
                                                                      -- BUT NOT ABOVE 25.
371
      00E2
             4F
                                      CLRA
                                                                              THEN--->
372
      00E3
             B7 23
                                      STA
                                               HYST
373
      00E5
             B7 21
                                      STA
                                               HYSTPT
374
                              ***
375
      00E7
             A6 00
                              DISPLA
                                      LDA
                                               #%00000000
                                                                  NO... JUST---->
376
      00E9
             B7 00
                                      STA
                                               PORTA
377
      00EB
             A6 C0
                                               #%11000000
                                      LDA
378
      OOED
             B7 01
                                      STA
                                               PORTB
379
                                                                        -- DISPLAY CURRENT 'HYST'.
380
      OOFF
             BE 21
                                      LDX
                                               HYSTPT
381
      00F1
             D6 03 BE
                                      LDA
                                               TABLE, X
382
      00F4
             B7 02
                                      STA
                                               PORTC
383
                                                                  IS 'HYST' SETTING COMPLETE?
384
      00F6
             09 03 C7
                                      BRCLR
                                               FUNCT, PORTD, CHHYST NO... KEEP CHECKING 'SET'.
385
      00F9
             08 25 05
                                      BRSET
                                               POSCT, STAT, SHOPOS YES... RESET THE DISPLAY.
386
      00FC
             CD 03 4E
                                      JSR
                                               OUTCT
387
      00FF
             20 03
                                      BRA
                                              DUNCHG
388
389
      0101
             CD 03 68
                              SHOPOS
                                      JSR
                                              OUTPOS
390
391
      0104
             OB 25 04
                              DUNCHG
                                     BRCLR
                                              FLASH, STAT, NO INT IF THE DISPLAY IS TO BLINK ...
```

392	0107	A6 07		LDA	#BIT2+BIT1+BIT0	ENABLE TIMER INTERRUPT AND RESET					
393	0109	B7 09		STA	TCR	TIMER PRESCALER					
394	010B	20 A5	NO_INT	BRA	PAUSE	PRIOR TO RETURNING.					
395			***								
396			**								
397			***************************************								
398			** MAXIMUM EXECUTION TIME FOR THE REMAINDER OF THE PROGRAM OCCURS								
399			** IF THE COUNTER ROTATES THROUGH ZERO AS THE DISPLAY MODE IS CHANGED								
400			** FROM	THE BLI	NKING MODE TO THE C	COUNT MODE AT THE SAME TIME THAT THE					
401			** BLINKING ROUTINE IS CAUSING THE DISPLAY TO TOGGLE TO SHOW THE								
402			** POSITION IN DEGREES.								
403			** MAXIMUM EXECUTION TIME = 140 + 184 + 708 = 1032 CLOCK CYCLES.								
404			***************************************								
405			**								
406			** MODE	CHANGE	ROUTINE. CHANGES T	HE DISPLAY MODE FROM					
407			**			IKING -> COUNT ->(ETC.)					
408			**			181 CLOCK CYCLES OCCURS WHEN THE					
409			**			ROM DISPLAYING THE COUNT TO DISPLAYING					
410			**		SITION (IN DEGREES)						
411			**		-	FROM BLINKING TO A COUNT DISPLAY					
412			**		ION TIME IS 140 CLC						
413			**								
414	0100	1F OA	CHMODE	BCLR	B7,MR	AVOID REPEATED INTERRUPTS.					
415			**								
416	010F	OA 25 10		BRSET	FLASH, STAT.DIS CT	IF FLASHING, DISPLAY COUNT					
417	0112	09 25 07		BRCLR		IF SHOWING COUNT, DISPLAY POSITION					
418	0115	1A 25		BSET	FLASH, STAT	ELSE, BLINK.					
419			**		· ·						
420	0117	A6 07		LDA	#BIT2+BIT1+BIT0	ENABLE TIMER INTERRUPT AND RESET					
421	0119	B7 09		STA	TCR	TIMER PRESCALER.					
422	011B	80		RTI							
423			**								
424	011C	18 25	DISPOS	BSET	POSCT, STAT						
425	011E	CD 03 68		JSR	OUTPOS	DISPLAY CURRENT POSITION, AND WAIT.					
426	0121	80		RTI							
427			**								
428	0122	A6 47	DIS_CT	LDA	#BIT6+BIT2+BIT1+BI	ITO DISABLE TIMER INTERRUPT AND RESET					
429	0124	B7 09		STA	TCR	TIMER PRESCALER.					
430	0126	19 25		BCLR	POSCT, STAT						
431	0128	1B 25		BCLR	FLASH, STAT						
432			**			DISPLAY CURRENT COUNT, AND WAIT.					
433	012A	CD 03 4E		JSR	OUTCT						
434	0120	80		RTI	••	·					
4 3 5			**								
436			*****	*****	******	*********					
437			**								
438						INE TO CHANGE THE DISPLAY FROM POSITION					
439			**			/ERY 31 ST TIMER INTERRUPT IF THE					
440			**	'FLASH	I' BIT OF 'STAT' IS	SET.					
441			**			184 CLOCK CYCLES OCCURS WHEN THE					
442			**	DISPLA	Y IS TOGGLED FROM A	COUNT DISPLAY TO A POSITION DISPLAY.					
443			**								
444		012E	BLINK	EQU	\$						
445	012E	OF 09 DC		BRCLR	TIR, TCR, CHMODE	IF THE INTERRUPT WAS NOT A TIMER					
446			**			INTERRUPT IT MUST BE FROM INT2.					
447			**								
448	0131	1F 09		BCLR	TIR,TCR	AVOID REPEATED TIMER INTERRUPTS.					
449			**								
450	0133	3A 27		DEC	TIMCT	IF THERE HAVE BEEN 31 TIMER					
451	0135	27 01		BEQ	CHGDIS	INTERRUPTS (1 SEC), IT'S TIME TO					
452			**			CHANGE THE DISPLAY.					
453	0137	80		RTI		OTHERWISE, IT'S BACK TO WORK.					
454			**								
455	0138	A6 1F	CHGDIS	LDA	#31	RESET TIMET TO 31 (1 SEC. INTERVAL).					
456	013A	B7 27	**	STA	TIMCT						
457			**								

```
458
      013C
             B6 25
                                       LDA
                                                STAT
                                                #%00010000
                                                                 |-- CHANGE 'POSCT' BIT OF 'STAT'.
      013E
             A8 10
                                       EOR
459
460
      0140
             B7 25
                                       STA
                                                STAT
461
             08 25 04
                                               POSCT, STAT, POSOUT
                                                                      DECIDE ON CORRECT DISPLAY.
462
      0142
                                       RRSET
463
                                              CHANGE THE DISPLAY TO SHOW THE COUNT.... ***********
                               *******
464
465
                               **
466
      0145
             CD 03 4E
                                       JSR
                                               OUTCT
467
      0148
             80
                                       RTI
468
                                             OR HAVE THE DISPLAY SHOW THE POSITION. ***********
469
                               *******
470
                               **
471
      0149
             CD 03 68
                               POSOUT
                                       JSR
                                                OUTPOS
472
      014C
             80
                                       RTI
473
474
475
                               **
                                                           COUNT ROUTINE.
476
                               **
477
                                         WHEN A COUNT IS RECEIVED THIS IS THE ENTRY POINT .
                               **
478
                                         MAXIMUM EXECUTION TIME OF 708 CLOCK CYCLES OCCURS WHEN THE
                               **
479
                                         COUNTER ROTATES CCW THROUGH ZERO AND THE POSITION (IN DEGREES)
480
                               **
                                         IS BEING DISPLAYED.
                               **
481
482
                               **
                               ** CURRENT DIRECTION OF ROTATION IS DETERMINED BY INSPECTING THE STATUS
483
484
                               ** OF 'CH A' AND 'CH B'. THE FOUR POSSIBILITIES AND THE ASSOCIATED
485
                               ** DIRECTION OF ROTATION ARE AS SHOWN BELOW. NOTE THAT THIS SCHEME
486
                               ** PREVENTS MULTIPLE OSCILLATIONS ABOUT A SINGLE POINT FROM
                               ** REPEATEDLY INCREMENTING OR DECREMENTING THE COUNTER.
487
488
                               **
489
490
                               **
                                       CH_A
                                                 CH_B
                                                           DIRECTION
                                                                              COUNT THE PULSE?
491
                               **
                                                           OF ROTATION
                               **
492
493
                               **
                                        LO
                                                  LO
                                                               CW
                                                                                     NO
494
                               **
                                        LO
                                                  ΗI
                                                               CCW
                                                                                     YES
495
                               **
                                                               CCW
                                        ΗI
                                                  LO
                                                                                     NO
                               **
496
                                        ΗI
                                                   ΗI
                                                               CW
                                                                                     YES
                               **
497
498
                               **
499
                               ****** FIRST SEE IF WE ARE SUPPOSED TO COUNT THIS INTERUPT. *******
                               **
500
501
             014D
                               COUNT
                                       EQU
502
      014D
             OA 03 01
                                       BRSET
                                                CH B, PORTD, OKCT
                                                                   IF CH B IS LO WE DON'T COUNT THE
503
      0150
             80
                                       RTI
                                                                   INTERRUPT.
504
505
                                       ****** IF THE INTERRUPT IS VALID UPDATE 'STAT'. **********
                               **
506
      0151
507
             A6 7F
                               OKCT
                                       LDA
                                                #%01111111
508
      0153
             B4 25
                                       AND
                                                STAT
                                                                SAVE ALL OF THE OLD 'STAT' EXCEPT THE
509
      0155
             B7 25
                                       STA
                                                                DIRECTION OF ROTATION.
                                                STAT
             A6 80
510
      0157
                                       LDA
                                                #%10000000
511
      0159
             B4 03
                                       AND
                                                PORTD
                                                                'CH A.PORTD' INDICATES THE DIRECTION
512
                                                                OF ROTATION AND BECOMES 'UD, STAT'.
513
      015B
             BA 25
                                       ORA
                                                STAT
                                                                ADD THE RESULTS TO GET
514
      015D
             B7 25
                                       STA
                                                STAT
                                                                THE NEW 'STAT'.
515
                               **
516
                                 DECIDE IF THE "SLACK" DUE TO BACKLASH/HYSTERESIS HAS BEEN TAKEN OUT.
517
518
      015F
             OE 25 09
                                       BRSET
                                               UD, STAT, HYSTCK IF ROTATING CW SEE BELOW.
519
      0162
             B6 24
                                       LDA
                                               HYSTCT
                                                                ELSE, SEE IF WE DECREMENT THIS TIME.
      0164
             27 60
520
                                       BEQ
                                                CCW
                                                                IF HYSTCT=0, GO TO THE COUNT DOWN
521
                                                                ROUTINE.
             A0 01
      0166
522
                                       SUB
                                                #1
                                                                ELSE, DECREMENT THE HYSTERESIS COUNTER.
523
      0168
             B7 24
                                       STA
                                               HYSTCT
```

524	016A	80		RTI		AND WAIT FOR THE NEXT INTERRUPT.
525			**			
526	016B	B6 23	HYSTCK	LDA	HYST	IF ROTATING CW
527	0160	B1 24	III OI CK	CMP	HYSTCT	AND HYST = HYSTCT
				-		
528	016F	27 03		BEQ	CM	COUNT THE PULSE .
529	0171	3C 24		INC	HYSTCT	ELSE, INCREMENT THE HYSTERESIS COUNTER,
5 30	0173	80		RTI		AND WAIT FOR ANOTHER PULSE.
531			**			
532			**			
533			*****	******	******	************
534			**			
			**			AND LICE BOUTING
535					CL	OCKWISE ROUTINE.
536			**			
537		0174	CW	EQU	\$	
538			**			
539			***			
540			******	*****	INCREMENT TH	E BINARY COUNTER (BINCT). ***********
541			***		INONE INCH II	is simult country (singly)
	047/	04.40				
542	0174	B6 12		LDA		IN AT THE LSB OF THE BINARY COUNTER.
543	0176	AB 01		ADD	#1 LOB1	IN = LOBIN + 1 ; CARRY -> C,CCR
544	0178	B7 12		STA	LOBIN	
545			***			
546	017A	B6 11		LDA	MIDBIN	
547	017C	A9 00		ADC	#0	ADD THE CARRY TO THE MIDDLE BYTE.
-						ADD THE CARRY TO THE MIDDLE BITE.
548	017E	B7 11		STA	MIDBIN	
549			***			
550	0180	B6 10		LDA	HIBIN	
551	0182	A9 00		ADC	#0	ADD THE CARRY TO THE HIGH BYTE.
552	0184	B7 10		STA	HIBIN	
553	0104	56	***	• • • • • • • • • • • • • • • • • • • •		

554						30
555				*****	TTT CLR/SET	MOD_32 APPROPRIATELY. *************
556			***			
557			***	THE FOL	LOWING SEVERA	AL LINES OF CODE ARE PRETTY MESSY. ALL THAT
558			***	IS BEIN	G DONE IS TO	ENSURE THAT THE SCALE FACTOR IS SET PROPERLY.
559			***	FOR THE	PAN AYIS THE	SCALE FACTOR IS;
560			***	TOK THE	170 70020 1111	. COMEL TACTOR 10)
			***		4 800	05 -> 0 007007 DE0DEFO
561			***		1 201	.SE => 0.007097 DEGREES
562			***			
563	0186	B6 12		LDA	LOBIN	IF THE LOW FIVE BITS OF 'LOBIN' ARE NOT
564	0188	A4 1F		AND	#%00011111	ZERO THEN THE NUMBER ISN'T A MODULO 32 NUMBER.
565	018A	26 OF		BNE	NOT 32	
566	018C	B6 11		LDA	MIDBIN	IF THE LOW SIX BITS OF 'MIDBIN' ARE ZERO
567		27 07				AND 'HIBIN' .NE. ZERO
	018E			BEQ	MOD	
568		A4 3F		AND	#%00111111	THEN THE NUMBER IS MODULO 16,384, AND WE
569	0192	26 03		BNE	MOD	DON'T WANT TO SET 'MOD_32,STAT', UNLESS
570	0194	00 11 04		BRCLR	B6, MIDBIN, NO	DT_32 THE NUMBER IS ALSO MODULO 32,768.
571			***		•	
572	0197	1C 25	MOD	BSET	MOD_32,STAT	
			MOU			
573	0199	20 02	***	BRA	DIRCHK	
574			***			
575	019B	1D 25	NOT_32	BCLR	MOD_32,STAT	
576			***			
577			***			
578	0190	B6 10	DIRCHK	I DA	HIBIN	
		2B 1D	DIKUIK			TE HIDIN - A LEADE POTATING COL TOURS
579	019F	25 10		BMI	CWNEG	IF HIBIN < 0 , WE'RE ROTATING CCW TOWARD
580			***			THE ORIGIN.
581			***			
582	01A1	26 14		BNE	CWPOS	
583	01A3	B6 11		LDA	MIDBIN	ELSE IF BINCT .NE. O
584	01A5	26 10		BNE	CWPOS	WE'RE ROTATING CW
585	01A7	B6 12		LDA	LOBIN	AWAY FROM THE ORIGIN.
586	01A9	26 OC		BNE	CWPOS	
587						
588			***			ELSE, WE'VE ROTATED CW THROUGH THE ORIGIN.
589	01AB	15 25		BCLR	NEGTIV, STAT	CLR NEGATIVE SIGN.

```
LDX
                                               #PTR4
590
      01AD
             AE 13
591
      01AF
             7F
                               CLRIT2 CLR
                                               , X
      0180
                                       INCX
                                                           -- RESET ALL COUNTERS AND DEGRES TO ZERO.
592
             5C
593
      01B1
             A3 1D
                                       CPX
                                               #THOUTH
                                               CLRIT2 --
594
      01B3
             23 FA
                                       BLS
                                               UPOUT
                                                             UPDATE OUTPUT.
      0185
             20 6B
                                       BRA
595
596
      01B7
             AD 74
                              CWPOS
                                       BSR
                                               ADDBCD
597
598
      01B9
             CD 02 6A
                                       JSR
                                               INCPOS
      01BC
             20 64
                                       BRA
                                               UPOUT
599
600
601
      01BE
             CD 02 CA
                              CWNEG
                                       JSR
                                               SUBBCD
             CD 02 6A
                                               INCPOS
602
     01C1
                                       JSR
603
     01C4
             20 5C
                                       BRA
                                               UPOUT
604
                              ---
605
                              **
                              ******************************
606
607
                              **
                               **
608
                                                    COUNTER-CLOCKWISE ROUTINE.
609
                               **
610
             0106
                              CCW
                                      EQU
611
                               **
                              ***
612
                               ********* CLR/SET MOD 32 APPROPRIATELY. ****************
613
                              ***
614
                              ***
615
                                      AGAIN SET THE SCALE FACTOR TO:
                              ***
616
                              ***
617
                                                      1 PULSE => 0.007097 DEGREES
                              ***
618
619
     0106
             B6 12
                                      LDA
                                               LOBIN
                                                            IF THE LOW FIVE BITS OF 'LOBIN' ARE NOT
620
     0108
             A4 1F
                                      AND
                                               #200011111
                                                            ZERO THEN THE NUMBER ISN'T A MODULO 32 NUMBER.
621
     01CA
             26 OF
                                      BNE
                                               NO 32
622
     01CC
             B6 11
                                               MIDBIN
                                                            IF THE LOW SIX BITS OF 'MIDBIN' ARE ZERO
                                      LDA
                                                            AND 'HIBIN' .NE. ZERO
623
     01CE
             27 07
                                      BEQ
                                               MODLO
624
     0100
             A4 3F
                                      AND
                                               #%00111111
                                                            THEN THE NUMBER IS MODULO 16,384, AND WE
                                                            DON'T WANT TO SET 'MOD_32, STAT', UNLESS
625
     0102
             26 03
                                      BNE
                                               MODLO
     0104
             00 11 04
                                      BRCLR
                                               B6, MIDBIN, NO 32 THE NUMBER IS ALSO MODULO 32,768.
626
                              ***
627
     0107
             1C 25
                                               MOD_32,STAT
628
                              MODLO
                                      BSET
629
     0109
             20 02
                                      BRA
                                               DECBIN
630
631
     01DB
                              NO 32
             1D 25
                                      BCLR
                                               MOD 32, STAT
632
                              ***
633
634
                              ******* DECREMENT THE BINARY COUNTER (BINCT). ***********
635
                              ***
636
     0100
             B6 12
                              DECBIN
                                               LOBIN
                                                       BEGIN AT THE LSB OF THE BINARY COUNTER.
                                      LDA
637
     01DF
             AO 01
                                       SUB
                                               #1
                                                       LOBIN = LOBIN - 1 ; BORROW -> C,CCR
             B7 12
638
     01E1
                                      STA
                                               LOBIN
639
640
      01E3
             B6 11
                                      LDA
                                               MIDBIN
641
     01E5
             A2 00
                                      SBC
                                                       SUBTRACT THE CARRY FROM THE MIDDLE BYTE.
                                               #0
642
     01E7
             B7 11
                                      STA
                                               MIDBIN
643
                              ***
644
      01E9
             B6 10
                                      LDA
                                               HIBIN
645
      01EB
             A2 00
                                      SBC
                                               #0
                                                       SUBTRACT THE CARRY FROM THE HIGH BYTE.
646
     01ED
             B7 10
                                       STA
                                               HIBIN
647
                              ***
             B6 10
648
      01EF
                                      LDA
                                               HIBIN
649
             2A 29
     01F1
                                      BPL
                                               CCWPOS
                                                             IF HIBIN .GE. 0 , WE'RE ROTATING CCW TOWARD
650
                                                             THE ORIGIN.
651
     01F3
             A6 FF
                                      LDA
                                               #-1
652
     01F5
             B1 10
                                       CMP
                                               HIBIN
653
      01F7
             26 1C
                                      BNE
                                               CCWNEG
                                                          -- ELSE IF BINCT .NE. -1
654
      01F9
             B1 11
                                      CMP
                                               MIDBIN
                                                          -- WE'RE ROTATING CCW AWAY
655
      01FB
             26 18
                                       BNE
                                               CCWNEG
                                                          -- FROM THE ORIGIN.
```

```
656
     01FD
            B1 12
                                     CMP
                                            LOBIN
                                            CCWNEG --
657
     O1FF
            26 14
                                     BNE
658
                                                          ELSE, WE'VE GONE THROUGH ORIGIN IN CCW
659
     0201
            14 25
                                    RSFT
                                            NEGTIV, STAT
                             ---
                                                          DIRECTION. SET NEGATIVE SIGN.
660
                             ***
661
                                                          AND SET ALL COUNTERS APPROPRIATELY.
     0203
                                            #03
662
           A6 03
                                     LDA
     0205
            B7 13
                                            PTR4
663
                                     STA
     0207
            B7 1A
                                            HUNDEG
                                                       -- DEGRES = 360.00
664
                                     STA
665
     0209
            A6 3C
                                     LDA
                                            #60
666
     020B
            B7 14
                                     STA
                                            PTR3
667
     0200
            AE 15
                                     LDX
                                            #PTR2
                                                    --
668
     020F
            7F
                             CLREM
                                     CLR
                                            , X
     0210
                                     INCX
                                                       -- EVERYTHING ELSE IS ZERO BEFORE CHANGE.
669
            5C
670
     0211
            A3 19
                                     CPX
                                            #CTPTR1 --
671
     0213
            23 FA
                                     BLS
                                            CLREM
672
                             ***
     0215
                                            ADDBCD
673
            AD 16
                             CCWNEG BSR
     0217
            CD 02 FD
                                     JSR
                                            DECPOS
674
675
     021A
            20 06
                                     BRA
                                            UPOUT
                             ***
676
677
     021C
            CD 02 CA
                             CCWPOS
                                    JSR
                                            SUBBCD
                                            DECPOS
            CD 02 FD
678
     021F
                                     JSR
679
680
                             ***
                             **
681
682
                             ***********************
683
                             **
684
                             ** OUTPUT ROUTINE. ROUTINE TO PRINT DATA TO THE OUTPUT PORTS. BY
685
                                     CALLING THE APPROPRIATE SUBROUTINE. ('OUTCT' TO OUTPUT THE
                             **
686
                                     THE COUNT AND 'OUTPOS' TO OUTPUT THE POSITION).
                             **
687
                             UPOUT EQU
688
            0222
689
                             **
            09 25 04
690
     0222
                                     BRCLR
                                           POSCT_STAT_PUTCT
691
692
     0225
            CD 03 68
                                     JSR
                                            OUTPOS
693
     0228
            80
                                     RTI
694
                             **
695
     0229
            CD 03 4E
                             PUTCT
                                     JSR
                                            OUTCT
696
     022C
            80
                                     RTI
697
                             ***************
698
699
                             ****** SUBROUTINE TO INCREMENT THE BCD COUNTER (BCDCT). *******
700
                             ***
701
     022D
            B6 19
                             ADDBCD LDA
                                            CTPTR1
            AB 01
702
     022F
                                     ADD
                                             #1
            A1 63
                                             #99
703
     0231
                                     CMP
                                                    CTPTR > 99 ?
            23 05
                                                    NO, WE'RE OK HERE. LOOK UP THE FIRST TWO DIGITS.
     0233
704
                                     RLS
                                            OK1
705
     0235
                                                    YES... MODIFY THE CTPTR,
            A0 64
                                     SHR
                                             #100
                                                    SET THE CARRY, AND
706
     0237
            99
                                     SEC
707
            20 01
     0238
                                     BRA
                                            OK1A
                                                    USE TABLE LOOK UP.
                             ***
708
                                                           NO CARRY EXISTS IF WE ENTER AT THIS POINT.
709
     023A
            98
                             OK1
                                     CLC
            B7 19
710
     023B
                                             CTPTR1 --
                             OK1A
                                     STA
     023D
            97
                                     TAX
711
712
                             ***
                                                        -- LOOK UP THE TWO LEAST SIGNIFICANT DIGITS.
     023E
            D6 03 BE
713
                                     LDA
                                             TABLE.X --
714
     0241
            B7 20
                                     STA
                                             TENONE --
715
     0243
            24 24
                                     BCC
                                             NOMO
                                                          AND CONTINUE ONLY IF THERE WAS A CARRY.
716
717
718
     0245
            B6 18
                                     LDA
                                            CTPTR2
            A9 00
719
     0247
                                     ADC
                                             #0
                                                    ADD THE CARRY.
     0249
            A1 63
                                     CMP
                                             #99
                                                    CTPTR > 99 ?
720
721
     024B
            23 05
                                     BLS
                                                    NO, WE'RE OK HERE. LOOK UP THE NEXT TWO DIGITS.
                                             OK2
```

```
#100
722
      0240
             A0 64
                                       SUR
                                                       YES... MODIFY THE CTPTR,
                                                       SET THE CARRY, AND
723
      024F
             99
                                       SEC
724
      0250
             20 01
                                               OK2A
                                                       USE TABLE LOOK UP.
                                       BRA
                               ***
725
      0252
                              OK2
                                                              NO CARRY EXISTS IF WE ENTER AT THIS POINT.
726
             98
                                       CLC
      0253
             B7 18
                                               CTPTR2
727
                              OK2A
                                       STA
728
      0255
             97
                                       TAX
729
                                                           -- LOOK UP THE NEXT TWO DIGITS IN THE TABLE.
730
      0256
             D6 03 BE
                                       LDA
                                               TABLE, X
731
      0259
             B7 1F
                                       STA
                                               HUNDRD --
      025B
                                               NOMO
                                                              AND CONTINUE ONLY IF THERE WAS A CARRY.
732
             24 OC
                                      BCC
                               ***
733
                                               CTPTR3
734
      025D
             B6 17
                                      LDA
                                      ADC
735
      025F
             A9 00
                                               #0
                                                             ADD THE CARRY.
             B7 17
736
      0261
                                       STA
                                               CTPTR3
737
      0263
             97
                                       TAX
738
                                                            -- LOOK UP THE NEXT TWO DIGITS IN THE TABLE.
739
      0264
             D6 03 BE
                                      LDA
                                               TABLE,X
740
      0267
             B7 1E
                                               TENTHO --
                                      STA
                              ***
741
742
     0269
             81
                              NOMO
                                      RTS
743
                              ***
744
                              ****** SUBROUTINE TO INCREMENT THE POSITION COUNTER (DEGRES). *******
745
746
                              ***
                               ***
747
                                    FIRST CHECK TO SEE IF THE BINARY COUNTER HAS REACHED A MODULO 32
                              ****
748
                                        NUMBER.
                              ****
749
750
      026A
             OD 25 04
                              INCPOS
                                      BRCLR
                                              MOD 32,STAT,INC7
                                                                  'MOD 32, STAT' SET ?
751
                              ***
      0260
752
             A6 08
                                      LDA
                                               #8
753
     026F
             20 02
                                      BRA
                                               INC
                                                              INCREMENT THE POSITION BY 0.008 DEGREES.
754
             A6 07
755
     0271
                              INC7
                                      LDA
                                               #7
                                                                   NO ....
756
     0273
             B7 22
                              INC
                                      STA
                                               POSINC
                                                              INCREMENT THE POSITION BY 0.007 DEGREES.
757
                              ****
758
                              **** ROUTINE TO INCREMENT THE POSITION COUNTER , 'DEGREES', BY A
                              ****
759
                                        PREDETERMINED AMOUNT, 'POSINC'.
                              ****
760
     0275
761
             B6 16
                                      LDA
                                               PTR1
     0277
             BB 22
                                               POSINC
762
                                      ADD
763
     0279
             A1 09
                                      CMP
                                                       PTR1 > 9 ?
                                               #9
764
     027B
             23 05
                                      BLS
                                               OK3
                                                       NO, WE'RE OK HERE. LOOK UP THE FIRST DIGIT.
765
     0270
             AO OA
                                      SUB
                                              #10
                                                       YES... MODIFY THE CTPTR.
                                                       SET THE CARRY, AND
766
      027F
             99
                                      SEC
767
     0280
             20 01
                                      BRA
                                               OK3A
                                                       USE TABLE LOOK UP.
                              ***
768
     0282
769
             98
                              OK3
                                      CLC
                                                              NO CARRY EXISTS IF WE ENTER AT THIS POINT.
             B7 16
      0283
770
                              OK3A
                                      STA
                                               PTR1
771
     0285
             97
                                      TAX
772
                                                           -- LOOK UP THE LEAST SIGNIFICANT DIGIT.
773
     0286
             D6 03 BE
                                      LDA
                                               TABLE.X
774
     0289
             87 1D
                                      STA
                                               THOUTH --
775
     0288
             24 3C
                                      BCC
                                               DONE
                                                              AND CONTINUE ONLY IF THERE WAS A CARRY.
776
                              ***
777
                              ****
     0280
             B6 15
778
                                      LDA
                                               PTR2
779
     028F
             A9 00
                                      ADC
                                               #0
                                                       ADD THE CARRY.
             A1 63
780
     0291
                                      CMP
                                               #99
                                                       PTR2 > 99 ?
781
     0293
             23 05
                                      BLS
                                              OK4
                                                       NO, WE'RE OK HERE. LOOK UP THE NEXT TWO DIGITS.
     0295
782
             A0 64
                                      SUR
                                               #100
                                                       YES ... MODIFY THE CTPTR,
783
     0297
             99
                                      SEC
                                                       SET THE CARRY,
784
     0298
             20 01
                                      BRA
                                              OK4A
                                                       AND USE TABLE LOOK UP.
785
                              ****
     029A
786
             98
                              OK4
                                      CLC
                                                              NO CARRY EXISTS IF WE ENTER AT THIS POINT.
787
     029B
             B7 15
                              OK4A
                                      STA
                                               PTR2
```

```
788
      0290
             97
                                     TAX
                              ****
                                                       -- LOOK UP THE NEXT TWO DIGITS IN THE TABLE.
789
      029E
                                             TABLE,X --
             D6 03 BE
790
                                     LDA
                                             HUNDTH --
791
      02A1
             B7 1C
                                     STA
            24 24
792
      02A3
                                     BCC
                                             DONE
                                                           AND CONTINUE ONLY IF THERE WAS A CARRY.
                              ****
793
                              ****
794
795
      02A5
             B6 14
                                     LDA
                                             PTR3
            A9 00
      02A7
                                                     ADD THE CARRY.
796
                                      ADC
                                             #0
                                             #99
797
      0249
             A1 63
                                      CHP
                                                     PTR3 > 99 ?
798
      02AB
             23 05
                                      BLS
                                             OK5
                                                     NO. WE'RE OK HERE. LOOK UP THE NEXT TWO DIGITS.
799
      02AD
             A0 64
                                      SUB
                                             #100
                                                     YES ... MODIFY THE CTPTR.
800
      02AF
             90
                                      SEC
                                                     SET THE CARRY, AND
            20 01
801
      02B0
                                             OK5A
                                                     USE TABLE LOOK UP.
                                      BRA
802
                             ****
803
      02B2
             98
                              OK5
                                      CLC
                                                           NO CARRY EXISTS IF WE ENTER AT THIS POINT.
804
      02B3
             B7 14
                              OK5A
                                     STA
                                             PTR3
805
      02B5
             97
                                     TAX
                              ****
806
                                                        -- LOOK UP THE NEXT TWO DIGITS IN THE TABLE.
807
      02B6
             D6 03 BE
                                     LDA
                                             TABLE, X
808
      02B9
             B7 1B
                                     STA
                                             ONEDEG --
809
      02BB
            24 OC
                                     BCC
                                             DONE
                                                           AND CONTINUE ONLY IF THERE WAS A CARRY.
                              ***
810
             B6 13
      02BD
                                     LDA
                                             PTR4
811
      02BF
            A9 00
                                     ADC
                                             #0
                                                     ADD THE CARRY.
812
813
      0201
             B7 13
                                     STA
                                             PTR4
814
      02C3
             97
                                     TAX
                              ****
815
                                                         -- LOOK UP THE NEXT TWO DIGITS IN THE TABLE.
      0204
             D6 03 BE
                                     LDA
816
                                             TABLE,X
                                             HUNDEG --
817
      0207
             B7 1A
                                     STA
                              ***
818
819
      0209
            81
                              DONE
                                     RTS
820
                              ***
                              **
821
                              ***********************************
822
823
                              ******* SUBROUTINE TO DECREMENT THE BCD COUNTER (BCDCT). *********
                              ***
824
825
            B6 19
      02CA
                              SUBBCD LDA
                                             CTPTR1
826
      0200
            A0 01
                                      SUB
                                             #1
                                                     CTPTR > 99 ?
            24 03
827
      02CE
                                     BCC
                                             OK6
                                                     NO, WE'RE OK HERE. LOOK UP THE FIRST TWO DIGITS.
      02D0
                                             #100
                                                     YES, MODIFY THE CTPTR, AND
828
            AB 64
                                     ADD
829
      02D2
            99
                                      SEC
                                                     GENERATE A BORROW.
                              ***
830
831
      02D3
            B7 19
                              OK6
                                     STA
                                             CTPTR1 --
      02D5
832
            97
                                     TAX
833
                              ***
                                                        -- LOOK UP THE TWO LEAST SIGNIFICANT DIGITS.
834
      0206
            D6 03 BE
                                      LDA
                                             TABLE,X --
835
      0209
            B7 20
                                     STA
                                             TENONE --
            24 1F
                                                        AND CONTINUE ONLY IF THERE WAS A BORROW.
836
      02DB
                                     RCC
                                             COMPLT
837
838
                              ***
839
      02DD
            B6 18
                                             CTPTR2
                                     LDA
840
      02DF
            A2 00
                                     SBC
                                             #0
                                                     SUBTRACT THE CARRY. CTPTR > 99 ?
      02E1
            24 03
841
                                     BCC
                                             OK7
                                                     NO, WE'RE OK HERE. LOOK UP THE NEXT TWO DIGITS.
842
     02E3
            AB 64
                                     ADD
                                              #100
                                                     YES, MODIFY THE CTPTR, AND
843
     02E5
            99
                                      SEC
                                                     GENERATE A BORROW.
844
                              ***
845
            B7 18
      02E6
                              OK7
                                     STA
                                             CTPTR2 --
846
     02E8
            97
                                      TAX
847
                              ***
                                                          -- LOOK UP THE NEXT TWO DIGITS IN THE TABLE.
848
     02E9
            D6 03 BE
                                     LDA
                                             TABLE,X
            B7 1F
849
     02EC
                                      STA
                                             HUNDRD --
850
     02EE
            24 OC
                                     BCC
                                             COMPLT
                                                           AND CONTINUE ONLY IF THERE WAS A CARRY.
851
                              ***
     02F0
            B6 17
                                             CTPTR3
852
                                     LDA
853
     02F2
            A2 00
                                                     SUBTRACT THE BORROW.
```

#0

SBC

```
854
      02F4
             B7 17
                                      STA
                                              CTPTR3 --
855
      02F6
             97
                                      TAX
                                                          -- LOOK UP THE NEXT TWO DIGITS IN THE TABLE.
856
                                              TABLE X --
             D6 03 BE
                                      LDA
857
      02F7
858
      02FA
             B7 1E
                                      STA
                                              TENTHO --
859
860
      02FC
             81
                              COMPLT RTS
                              ***
861
                              *******************************
862
                              ****** SUBROUTINE TO DECREMENT THE POSITION COUNTER (DEGRES). ******
863
                              ***
864
                              ***
                                    FIRST CHECK TO SEE IF THE BINARY COUNTER HAS REACHED A MODULO 32
865
                              ***
                                       NUMBER.
866
867
                              ***
      02FD
             00 25 04
                              DECPOS BRCLR
                                              MOD 32, STAT, DEC7
                                                                      'MOD 32, STAT' SET ?
868
869
                              ***
             A6 08
870
      0300
                                      LDA
                                              #8
                                                                      YES...
871
      0302
             20 02
                                      BRA
                                              DEC
                                                             DECREMENT THE POSITION BY 0.008 DEGREES.
                              ****
872
873
      0304
             A6 07
                              DEC7
                                      LDA
                                                                      NO ....
      0306
             B7 22
                                                             DECREMENT THE POSITION BY 0.007 DEGREES.
874
                              DEC
                                      STA
                                              POSINC
875
                              ****
                              **** ROUTINE TO DECREMENT THE POSITION COUNTER ,'DEGREES', BY A
876
                              ***
877
                                       PREDETERMINED AMOUNT, 'POSINC'.
                              ***
878
      0308
             B6 16
                                      LDA
879
                                              PTP1
880
      030A
             BO 22
                                      SUR
                                              POSINC PTR1 < 0 ?
                                                      NO, WE'RE OK HERE. LOOK UP THE FIRST DIGIT.
881
      030C
             24 03
                                      BCC
                                              OK8
882
      030E
             AB OA
                                                      YES, MODIFY THE CTPTR, AND
                                      ADD
883
      0310
             99
                                      SEC
                                                      GENERATE A BORROW.
884
                              ***
885
             B7 16
      0311
                              OK8
                                      STA
                                              PTR1
886
      0313
             97
                                      TAX
887
                                                         -- LOOK UP THE LEAST SIGNIFICANT DIGIT.
888
      0314
             D6 03 BE
                                      LDA
                                              TABLE,X --
889
      0317
             B7 1D
                                              THOUTH --
                                      STA
890
      0319
             24 32
                                      BCC
                                              DUNSUB
                                                           AND CONTINUE ONLY IF THERE WAS A BORROW.
                              ***
891
                              ***
892
893
      031B
             B6 15
                                      LDA
                                              PTR2
894
      031D
             A2 00
                                      SBC
                                              #0
                                                      SUBTRACT THE BORROW. PTR2 < 0 ?
895
      031F
             24 03
                                      BCC
                                              OK 9
                                                      NO, WE'RE OK HERE. LOOK UP THE NEXT TWO DIGITS.
896
      0321
             AB 64
                                      ADD
                                              #100
                                                      YES, MODIFY THE CTPTR, AND
897
             99
      0323
                                      SEC
                                                      GENERATE A BORROW.
898
                              ***
      0324
899
             B7 15
                              OK9
                                      STA
                                              PTR2
900
      0326
             97
                                      TAX
901
                                                         -- LOOK UP THE NEXT TWO DIGITS IN THE TABLE.
902
      0327
             D6 03 BE
                                      LDA
                                              TABLE,X --
903
      032A
             B7 1C
                                      STA
                                              HUNDTH --
             24 1F
904
      032C
                                      BCC
                                              DUNSUB
                                                           AND CONTINUE ONLY IF THERE WAS A CARRY.
905
906
                              ***
907
      032E
             B6 14
                                      LDA
                                              PTR3
908
      0330
             A2 00
                                      SBC
                                              #0
                                                      SUBTRACT THE BORROW. PTR3 < 0 ?
909
      0332
             24 03
                                      BCC
                                              OK10
                                                      NO, WE'RE OK HERE. LOOK UP THE NEXT TWO DIGITS.
910
      0334
             AB 64
                                      ADD
                                              #100
                                                      YES, MODIFY THE CTPTR, AND
911
      0336
             99
                                      SEC
                                                      GENERATE A BORROW.
912
913
      0337
             B7 14
                                              PTR3
                              OK10
                                      STA
914
      0339
             97
                                      TAX
915
                              ****
                                                           -- LOOK UP THE NEXT TWO DIGITS IN THE TABLE.
916
      033A
             D6 03 BE
                                      LDA
                                              TABLE, X --
917
      033D
             B7 1B
                                      STA
                                              ONEDEG --
             24 OC
918
      033F
                                      BCC
                                              DUNSUB
                                                           AND CONTINUE ONLY IF THERE WAS A CARRY.
919
```

```
LDA
                                              PTR4
920
      0341
             B6 13
      0343
             A2 00
                                      SBC
                                               #0
                                                      SUBTRACT THE BORROW.
921
                                              PTR4
             B7 13
922
      0345
                                      STA
923
      0347
             97
                                      TAX
924
                                                            -- LOOK UP THE NEXT TWO DIGITS IN THE TABLE.
                                               TABLE,X
925
      0348
             D6 03 BE
                                      LDA
             B7 1A
                                      STA
                                               HUNDEG --
926
      034B
927
     034D
                              DUNSUB
             81
                                      RTS
928
929
930
                              **
                              **
931
                              932
                              **
933
934
                                 OUTPUT COUNT (OUTCT). SUBROUTINE TO MOVE THE CURRENT COUNT (BCDCT)
                              **
935
                                       TO THE OUTPUT PORTS. REMOVES THE DECIMAL POINT FROM THE
                              **
                                       DISPLAY AND BLANKS ALL BUT THE LEAST SIGNIFICANT DIGIT. ALSO
936
937
                              **
                                       SETS THE MINUS SIGN IF APPROPRIATE.
                              **
938
                                      EQU
939
             034E
                              OUTCT
940
941
      034E
             B6 20
                                      LDA
                                               TENONE
942
      0350
             B7 02
                                               PORTC
                                      STA
943
                                      LDA
944
      0352
             B6 1F
                                               HUNDRD
                                               PORTA
945
      0354
             B7 00
                                      STA
946
947
      0356
             B6 1E
                                      LDA
                                               TENTHO
             B7 01
                                               PORTB
948
      0358
                                      STA
949
950
             1E 01
                                      BSET
                                               DECPT, PORTB
      035A
                                               BLANK, PORTB
951
             19 01
                                      BCLR
      035C
952
953
      035F
             04 25 04
                                      BRSET
                                               NEGTIV, STAT, MINUS
                                               POSTIV, PORTB
954
      0361
             1C 01
                                      BSET
      0363
             20 02
                                      BRA
                                               ALLDUN
955
956
                               **
957
      0365
                                      BCLR
                                               POSTIV, PORTB
             1D 01
                              MINUS
958
959
      0367
             81
                               ALLDUN
                                      RTS
                              **
960
961
                               ** OUTPUT POSITION (OUTPOS). SUBROUTINE TO MOVE THE CURRENT POSITION
962
                               **
                                       COUNT (BCDCT) TO THE OUTPUT PORTS. THE DECIMAL POINT IS
963
964
                               **
                                       DISPLAYED , AND ONLY THE MOST SIGNIFICANT DIGIT IS BLANKED.
965
                               **
966
             0368
                              OUTPOS EQU
967
                               **
968
      0368
             B6 1D
                                       LDA
                                               THOUTH
969
      036A
             A1 05
                                       CMP
                                               #5
                                                               IF 5 > 'THOUTH' SIMPLY TRUNCATE THE
      036C
             25 38
970
                                       BLO
                                               TRUNC
                                                             -- DISPLAY. OTHERWISE..
971
      036E
             B6 1C
                                               HUNDTH
                                       LDA
972
             A4 09
                                               #9
                                                             -- IF THE LAST DIGIT ISN'T A NINE IT IS
      0370
                                       AND
             A1 09
                                                             -- EASY TO ROUND UP. JUST ADD A ONE.
973
      0372
                                       CMP
                                               #9
                                               DECIMAL
974
      0374
             26 28
                                       BNE
975
      0376
             B6 1C
                                       LDA
                                               HUNDTH
                                                             -- BUT IF THE LAST DIGIT IS A NINE CHECK TO
             A1 99
                                                             -- SEE IF IT'S 99. IF SO IT GETS GRIM.
976
      0378
                                       CMP
                                               #599
             27 04
977
                                       BEQ
      037A
                                               UGLY
978
             AB 07
                                       ADD
                                               #7
                                                             -- IF THE NUMBER IS X9 AND X .NE. 9, THEN
      037C
                                                             -- JUST ADD SEVEN TO ROUND UP. DUE TO
979
      037E
             20 28
                                       BRA
                                               PCOUT
980
                               **
                                                             -- HEXIDECIMAL.
                               **
981
                                                             -- IF THE LOW TWO DIGITS ARE BOTH NINES
      0380
                                                               AND WE NEED TO ROUND UP....
982
             A6 00
                               UGLY
                                       LDA
                                               #00
                                                                MAKE THE LOW TWO DIGITS BOTH ZEROS
983
      0382
             B7 02
                                       STA
                                               PORTC
984
      0384
             99
                                       SEC
                                                                AND SET THE CARRY.
985
```

```
986
       0385
              B6 1B
                                        LDA
                                                ONEDEG --
                                                                  CHECK THE LAST DIGIT AS BEFORE.
              A4 09
                                                #9
                                                                  IF USING THIS PORTION OF THE CODE
 987
       0387
                                        AND
                                                 #9
                                                                  THERE HAD TO BE A CARRY.
 988
       0389
              A1 09
                                        CMP
                                                               -- IF THE LAST DIGIT IS NOT A NINE USE THE
       0388
                                                NEXT
 989
              26 1E
                                        BNE
 990
       0380
              B6 1B
                                                ONEDEG
                                                               -- ADC INSTRUCTION BELOW.
                                        LDA
 991
       038F
              A1 99
                                        CMP
                                                 #$99
                                                               -- IF IT IS A NINE, IS THE NEXT ONE A NINE
 992
       0391
              27 04
                                        BEQ
                                                 RLUGLY
                                                               -- ALSO?
 993
       0393
              AB 07
                                        ADD
                                                 #7
                                                                  IF NOT JUST ADD SEVEN,
                                                                  AND DISPLAY THE OUTPUT.
 994
       0395
              20 18
                                        BRA
                                                PAOUT
                                                          - -
995
              A6 00
996
       0397
                                RLUGLY
                                                 #00
                                        LDA
              B7 00
                                                                  IF SO ROUND UP THE MOST SIGNIFICANT
997
       0399
                                        STA
                                                PORTA
                                                            --
998
                                                            - -
                                                                  DIGIT AND SET EVERYTHING ELSE TO ZERO.
       039B
              99
                                        SEC
999
              20 13
                                        BRA
                                                NEXT1
       039C
                                **
1000
              B6 1C
                                DECIMAL LDA
1001
       039E
                                                 HUNDTH --
1002
      03A0
              AB 01
                                        ADD
                                                 #1
1003
                                                                  THIS IS ALL THAT NEEDS TO BE DONE IF
1004
       03A2
              B7 02
                                        STA
                                                PORTC
                                                                  THE LAST DIGIT IS NOT A NINE.
1005
       03A4
              20 05
                                        BRA
                                                NEXT
1006
                                **
1007
       03A6
              B6 1C
                                TRUNC
                                        LDA
                                                HUNDTH
                                                          -- AND IF THERE IS NO CARRY IT'S EVEN EASIER.
1008
       03A8
              B7 02
                                PCOUT
                                        STA
                                                PORTC
1009
       03AA
              98
                                        CLC
1010
                                **
1011
       03AB
              B6 1B
                                NEXT
                                        LDA
                                                ONEDEG
              A9 00
1012
       03AD
                                        ADC
                                                #0
1013
       03AF
              B7 00
                                PAOUT
                                        STA
                                                PORTA
1014
1015
       03B1
              B6 1A
                                NEXT1
                                        LDA
                                                HUNDEG
                                        ADC
              A9 00
                                                #0
1016
       03B3
              B7 01
                                                PORTB
1017
       03B5
                                        STA
1018
1019
       03B7
              10 01
                                        BSET
                                                POSTIV, PORTB
1020
       03B9
              18 01
                                        BSET
                                                BLANK, PORTB
              1F 01
                                                DECPT, PORTB
1021
       03BB
                                        BCLR
1022
                                **
1023
       03BD
              81
                                        RTS
1024
                                **
1025
                                **
1026
                                ************************************
1027
1028
                                ** SET UP THE TABLE TO BE USED WITH BCD INCREMENT/DECREMENT ROUTINES.
                                **
1029
1030
                                        ENDS
1031
                                        DATA
1032
       03BE
              00 01 02 03 04
                                TABLE
                                        FCB
                                                $00,$01,$02,$03,$04,$05,$06,$07,$08,$09
              05 06 07 08 09
       03C3
1033
       03C8
              10 11 12 13 14
                                        FCB
                                                $10,$11,$12,$13,$14,$15,$16,$17,$18,$19
       03CD
              15 16 17 18 19
1034
       0302
              20 21 22 23 24
                                        FCB
                                                $20,$21,$22,$23,$24,$25,$26,$27,$28,$29
       0307
              25 26 27 28 29
1035
       03DC
              30 31 32 33 34
                                        FCB
                                                $30,$31,$32,$33,$34,$35,$36,$37,$38,$39
       03E1
              35 36 37 38 39
1036
       03E6
              40 41 42 43 44
                                        FCB
                                                $40,$41,$42,$43,$44,$45,$46,$47,$48,$49
              45 46 47 48 49
       03EB
1037
              50 51 52 53 54
       03F0
                                        FCB
                                                $50,$51,$52,$53,$54,$55,$56,$57,$58,$59
       03F5
              55 56 57 58 59
1038
       03FA
              60 61 62 63 64
                                        FCR
                                                $60,$61,$62,$63,$64,$65,$66,$67,$68,$69
       03FF
              65 66 67 68 69
1039
       0404
              70 71 72 73 74
                                        FCB
                                                $70,$71,$72,$73,$74,$75,$76,$77,$78,$79
       0409
              75
                 76 77 78 79
1040
       040E
              80
                 81 82 83 84
                                        FCB
                                                $80,$81,$82,$83,$84,$85,$86,$87,$88,$89
       0413
              85 86 87 88 89
       0418
              90 91 92 93 94
1041
                                        FCB
                                                $90,$91,$92,$93,$94,$95,$96,$97,$98,$99
              95 96 97 98 99
       041D
```

1042			*	ENDS		
1043			*	CODE		
1044			*****	*****	******	***********
1045			**			
1046			**			SET UP MASK OPTION REGISTER.
1047			**			
1048	0422			ABSOLU1	TE	
1049			**			
1050			**			
1051	0F38			ORG	MOR	
1052	0F38	07		FCB	#BIT2+B	IT1+BITO
1053		•	**			
1054			**	COMMENT	rs:	
1055			**	BIT 7		OURCE 0 = CRYSTAL.
1056			**	BIT 6		PTION 0 = INTERNAL.
1057			**	BIT 5		LOCK SOURCE 0 = INTERNAL.
1058			**	BIT 4	NOT USE	
1059			**	BIT 3	NOT USE	
1060			**	BIT 2	SET -	••
1061			**	BIT 1		- PRESCALE SELECT 111 => 128
1062			**	BIT O	SET -	THE OWNER OF THE TENT
1063			**	••••		
1064			**			
1065			*****	*****	******	*************
1066			**			
1067			**			ASSIGN INTERRUPT VECTORS.
1068			**			Monay Internal Tenanol
1069	OFF8			ORG	INTRPT	
1070	0110		**		214170. 1	
1071	OFF8	012E		FDB	BLINK	TIMER/INT2 INTERRUPT VECTOR.
1072	OFFA	014D		FDB	COUNT	
1073	OFFC	014D		FDB	COUNT	
1074	OFFE	0080		FDB	RESTRT	•
1075	0112	0000	**	, 55	KEO!K!	NGOLI VLOTONI
1076			**			
1077			**			
1077				ENDS		
1079	1000			END		
1017	1000			CHU		

Lines Assembled: 1079 Assembly Errors: 0

```
POSITION DETERMINING PROGRAM (ELEVATION)
                                         TTL
 2
                                                         LATEST REVISION
                                                                                        9 MAY 89
 3
                                                         FILE NAME
                                                                                        TILT.ASM
 4
 5
                                   PROGRAM DESCRIPTION
 6
                                **
 7
                                **
                                **
 8
 9
                                   I/O REGISTER ADDRESSES
10
                                                  $0000
11
             0000
                                PORTA
                                         EQU
                                                          I/O PORT A
             0001
                                PORTB
                                         EQU
                                                  $0001
                                                           I/O PORT B
12
13
             0002
                                PORTC
                                         EQU
                                                  $0002
                                                           I/O PORT C
                                                  $0003
                                                           INPUT PORT D
14
             0003
                                PORTD
                                         EQU
15
                                ** DATA DIRECTION REGISTER OFFSET
16
                                **
17
18
             0004
                                DDR
                                         EQU
                                                          (eg. DDR FOR PORT A IS PORTA+DDR )
19
                                ** OTHERS
20
                                **
21
22
             8000
                                TIMER
                                         EQU
                                                  $0008
                                                          EIGHT BIT TIMER REGISTER.
                                                  $0009
23
             0009
                                TCR
                                         FOU
                                                          TIMER CONTROL REGISTER.
24
             000A
                                MR
                                         EQU
                                                  $000A
                                                          MISCELLANEOUS REGISTER.
25
             0010
                                RAM
                                         EQU
                                                 $0010
                                                          START OF ON-CHIP RAM(112 - 31 FOR STACK)
                                                          PAGE ZERO OF ROM.
26
             0080
                                ZROM
                                         EQU
                                                 $0080
27
             0100
                                ROM
                                         EQU
                                                 $0100
                                                          START OF HAIN ROM.
28
             0F38
                                MOR
                                         FOU
                                                 $0F38
                                                          MASK OPTION REGISTER.
29
             OFF8
                                INTRPT
                                        EQU
                                                 SOFF8
                                                          LOCATION OF INTERRUPT VECTORS.
30
             1000
                                MEMSIZ EQU
                                                 $1000
                                                          MEMORY ADDRESS SIZE.
31
                                ** EQUATES
32
                                **
33
             0001
                                BITO
                                                  1
34
                                        EQU
35
             0002
                                BIT1
                                        EQU
                                                 2
36
             0004
                                        EQU
                                                 4
                                BIT2
37
             0008
                                BIT3
                                        EQU
                                                 8
38
             0010
                                        E QU
                                BIT4
                                                 16
39
             0020
                                BIT5
                                        EQU
                                                 32
40
             0040
                                B116
                                        EQU
                                                 64
41
             0080
                                BIT7
                                        EQU
                                                  128
42
                                **
43
             0000
                                B0
                                        EQU
                                                 0
44
             0001
                                В1
                                        EQU
                                                 1
45
             0002
                                B2
                                        EQU
                                                 2
46
             0003
                                В3
                                                 3
                                        EQU
47
             0004
                                B4
                                        EQU
                                                 4
             0005
48
                                B5
                                        EQU
                                                 5
49
             0006
                                B6
                                        EQU
                                                 6
50
             0007
                                B7
                                        EQU
51
                                **
52
                                ** EQUATES FOR THE TIMER CONTROL REGISTER
53
                                **
54
                                ***
55
             0007
                                TIR
                                        EQU
                                                          TIMER INTERRUPT REQUEST. 1 = REQUEST, 0 = NO REQ.
56
             0006
                                TIM
                                        EQU
                                                 6
                                                          TIMER INTERRUPT MASK. 1 = DISABLED, 0 = ENABLED.
57
             0005
                                                          EXTERNAL OR INTERNAL CLOCK SOURCE. 1 = EXT, 0 = INT.
                                        EQU
                                                 5
                                TIN
58
             0004
                               TEE
                                        EQU
                                                 4
                                                          EXTERNAL CLOCK ENABLE. NOT USED.
59
             0003
                               PSC
                                        EQU
                                                 3
                                                          PRESCALER CLEAR. NOT USED.
60
             0002
                                PS2
                                        EQU
                                                 2
                                                          (PS2)
61
             0001
                               PS<sub>1</sub>
                                        EQU
                                                          (PS1)
                                                                   -- PRESCALER SELECT BITS.
```

45	0000									
62 63	0000	PS0	EQU	0	(PSO) -	-				
64		** EQUA	TES FOR	THE STAT	US BYTE,	'STAT'.				
65		***								
66		***								
67 68	0007	UD	EQU	7	COUNT DI	PECTION2	1 = 110	0 = 00	JN.	
69	0006	MOD 32	====	,						
70	0005	FLASH	EQU	5	IS 'BINC'	E DISPLA	Y? $1 = Y$	ES, 0 =	NO.	
71	0004	POSCT	EON EON EON EON	4	DISPLAY I	POSITION	OR COUNT	? 1 = 1	POS, 0 =	COUNT.
72 73	0003 0002	L_SET NEGTIV	EQU	3	IS BCDC.	MODE,P	ORTD' LAS	T TIME.	VFC 0 -	NO
74	0002	### MEGITA	EWO	1	NOT USED		VC NUMBER	r 1 =	123, 0 -	MU.
75		***		0	NOT USED					
76		***								
77		***	FOUNTEC	AND DECC	2017770					
78 79		***	EMUATES	AND DESC	RIPTIONS.					
80		***								
81		***	PORT /	(1/0)						
82		***								
83 84		***	1		nicit #/					
85		***	+		DIGIT #4					
86		***	D4	C4	B4	A4	D3	C3	B3	A3
87		***			-+	+	++		++	
88 89		*** BIT	7	6	5	4	3	2	1	0
90		***								
91		***	PORT E	(1/0)						
92		***								
93		***			-+					
94 95		***	1	DISPLA	Y CONTROL	.	 	NOI	USED	
96		***			v				l i	
97		***	+			+				
98		*** BIT	7	6	5	4	3	2	1	0
99 100	0007	***	FOU	7	TO DISPL	AV TUE N		THE D	CODT 10 0	TA OFF
100	0007	DECPT POSTIV			USED TO I					
102	••••	***			MINUS SI			0.0		C Cilow
103	0004	BLANK	EQU	4	TO BLANK					
104		***					RE ALWAYS		D.	
105 106		***			DIGII 1	IS NEVER	BLANKED.			
107		***	PORT ((1/0)						
108		***								
109		***	+		-+					
110 111		***	1	BCD	DIGIT #2	.	IRCO DIGI	1 #1(LE	ASI SIGNI	FICANI)
112		***			B2					
113		***	+			+			+	+
114		*** BIT	7	6	5	4	3	2	1	0
115 116		***								
117		***	PORT D	(INPUT	ONLY)					
118		***		(,					
119		***			-+				++	+
120		***	CH_A	I INT2	CH_B	FUNCT	SET			
121 122		*** BIT	7	6	5	44	3	2	+ 1	0
123		***	'			•	,			The state of the s
124	0007	CH_A	EQU	7	INDICATE	S THE ST	ATUS OF C	HANNEL	A.	
125	0006	INT2	EQU	6	INTERRUP	T #2. U	SED TO CH	ANGE DI	SPLAY MOD	ES.
126 127	0005 0004	CH_B FUNCT	EQU EQU	-	USED TO					II ALLOS
127	0004	FUNCT	EWU	4	ו טובט וטו	FUI INE I	FROGRAM I	n A HUU	c inal WI	LL ALLOW

```
'HYST' TO BE INCREMENTED.
128
129
            0003
                             SET
                                     FOU
                                             3
                                                     INCREMENTS 'HYST' WHEN TOGGLED AND FUNCT IS LOW.
130
                             ***
131
                             ***
                                     -----
                             ****
132
                             **
133
                             **
                                                        RAM VARIABLES
134
135
                                        136
137
138
                             ** RESERVE MEMORY SPACE FOR THE PROGRAM VARIABLES.
139
                             **
140
     0000
                                     DATA
                             **
141
142
                             **
143
     0000
                                     ABSOLUTE (ABSOLUTE ADDRESSING USED HERE TO RELATIVE DIRECTIVE)
144
145
     0010
                                     ORG
                                             RAM
                                                     START OF RAM.
                             **
146
                             *** BINARY COUNT.
147
148
     0010
                                     RMB
                                             2
                             BINCT
                                     EQU
149
                             HIBIN
                                             BINCT
                                                     HI BYTE.
            0010
150
            0011
                             LOBIN
                                     EQU
                                             BINCT+1 LO BYTE.
151
                             **
152
                             *** POSITION POINTERS.
153
     0012
                             PTR
                                     RMB
                                             3
                                                     EACH BYTE POINTS TO A POSITION IN THE
154
                             **
                                                     TABLE THAT CONTAINS ONE OR TWO DIGITS
                             **
                                                     OF THE BCD POSITION.
155
                                     EQU
                                              PTR
                             PTR3
                                                     MOST SIGNIFICANT DIGITS.
156
            0012
157
            0013
                             PTR2
                                     EQU
                                              PTR+1
158
            0014
                             PTR1
                                     EQU
                                              PTR+2 LEAST SIGNIFICANT DIGIT.
                             **
159
                             *** COUNT POINTERS.
160
     0015
                                             2
                                                     EACH BYTE POINTS TO A POSITION IN THE
161
                             CTPTR
                                    RMB
                             **
                                                     TABLE THAT CONTAINS TWO OF THE DIGITS
162
                             **
163
                                                     IN THE BCD COUNT.
                                             CTPTR
            0015
                             CTPTR2 EQU
                                                     MOST SIGNIFICANT DIGITS.
164
165
            0016
                             CTPTR1 EQU
                                             CTPTR+1 LEAST SIGNIFICANT DIGITS.
166
                             **
                             *** BCD POSITION IN DEGREES.
167
168
     0017
                             DEGRES RMB
                                             3
169
            0017
                             ONEDEG EQU
                                             DEGRES
                                                          CONTENTS X
                                                                       1.000
            0018
                             HUNDTH EQU
170
                                             DEGRES+1
                                                          CONTENTS X
                                                                       0.010
171
            0019
                             THOUTH EQU
                                             DEGRES+2
                                                         + CONTENTS X
                                                                       0.001
172
173
                             ***
                                                          POSITION IN DEGREES
                             **
174
175
                             *** BCD COUNT.
     001A
                                             2
176
                             BCDCT
                                    RMB
177
            001A
                             HUNDRD EQU
                                             BCDCT
                                                                         100
                                                          CONTENTS X
178
            001B
                             TENONE EQU
                                             BCDCT+1
                                                         + CONTENTS X
                             ***
179
                             ***
180
                                                        NUMBER OF PULSES COUNTED
181
                             ***
182
                             *** HYSTERESIS COUNTER. POINTS TO A NUMBER IN THE TABLE THAT IS THE
183
                                     AMOUNT OF HYSTERESIS PRESENT IN THE SYSTEM. INITIALIZED TO 6.
184
     001C
                             HYSTPT RMB
                                              1
185
                             **
                             *** POSITION INCREMENT. CONTAINS A NUMBER, THAT WHEN MULTIPLIED BY 0.001
186
187
                             ***
                                     IS THE NUMBER OF DEGREES THAT THE POSITION COUNTER (BCDPOS) IS
                             ***
188
                                      TO BE INCREMENTED OR DECREMENTED DURING PROGRAM EXECUTION.
189
                             ***
                                     THE VALUE OF 'POSINC', DETERMINED EXPERIMENTALLY, SHOULD BE
190
                             ***
                                     7.0452. SINCE THE PROGRAM IS DESIGNED WORK WITH INTEGERS ONLY
                             ***
191
                                     THIS NUMBER IS ROUNDED TO 7. TO REDUCE THE CUMULATIVE EFFECT OF
                             ***
                                     THE ROUND OFF, EVERY 32 COUNTS 'POSINC' IS SET EQUAL TO 8. THIS
192
193
                             ***
                                     AGAIN LEADS TO SOME CUMULATIVE ERROR, BUT THE SMALL ANGULAR RANGE
```

```
194
                              +++
                                       OF THE TILT ANGLE (10.5 DEGREES) ALLOWS US TO NEGLECT ANY FURTHER
                              ***
195
                                       MODIFICATIONS.
                              ***
196
      0010
197
                              POSINC RMB
                                            - 1
198
                              ***
199
                              *** HYSTERESIS VARIABLES. USED TO ELIMINATE THE EFFECTS OF BACKLASH ON
200
                              ***
                                       THE POSITION MEASUREMENTS.
201
                              ***
                                                      THE THRESHHOLD VALUE DETERMINED
202
      001E
                              HYST
                                      PMR
203
                              ***
                                                      EXPERIMENTALLY.
                                                      CURRENT AMOUNT OF HYSTERESIS MEASURED.
204
      001F
                              HYSTCT
                                      RMB
205
                              ***
                              *** STATUS BYTE. USED TO KEEP TRACK OF WHAT IS GOING ON.
206
                              ***
207
208
      0020
                              STAT
                                              1
                                                      CURRENT STATUS.
                                      RMR
209
      0021
                              LSTAT
                                      RMB
                                              1
                                                      PREVIOUS/LAST STATUS. USED TO KEEP TRACK OF
210
                              ***
                                                      L SET ONLY.
                              ***
211
                              *** TIMER COUNTER. USED IN CONJUNCTION WITH THE TIMER PRESCALER AND THE
212
                              ***
                                       TOR TO KEEP TRACK OF ONE SEC. INTERVALS. USED IN BLINKING THE
213
                              ***
                                       DISPLAY. INITIALLY SET TO 31, WHEN THE 'FLASH' BIT OF 'STAT'
214
                              ***
                                       IS SET. TIMCT IS DECREMENTED EACH CLOCK INTERRUPT (APPROX. 31
215
                              ***
                                       TIMES PER SEC). RESET TO 31 WHEN CONTENTS GO TO ZERO.
216
                              ***
217
                                       WHEN (TIMCT)=0 THE DISPLAY WILL TOGGLE.
                              ***
218
      0022
                                      RMB
219
                              TIMCT
220
221
                                      ENDS
                              **
222
                              ***
223
                              *****
224
                              **
225
                              **
                                                        PAGE ZERO ROM
226
                              --
227
                              ******************
228
                              **
229
                              **
                                                    INITIALIZATION ROUTINE.
230
                              **
231
232
                              **
233
      0000
                                      CODE
234
                              **
235
      0800
                                      ORG
                                              ZROM
                                                      PAGE ZERO ROM.
236
237
      0080
                                                      RELATIVE ADDRESSING MUST BE USED FOR THE BRANCH.
                                      RELATIVE
238
                              **
239
             0080
                                                      THIS IS THE ENTRY POINT WHEN AN EXTERNAL
                              RESTRT
                                      FOU
                              ***
240
                                                      INTTERRUPT OCCURS.
                              **
241
                              **********************************
242
                              **
243
                              ***
244
                                               INITIALIZE THE PC AND CLEAR RAM.
245
                              ***
                              ***
246
247
      0800
             9B
                                                      SET INTERUPT TO AVOID INTERUPTION AND
                                      SEI
                                                      RESET THE STACK POINTER. JUST IN CASE!
248
      0081
             90
                                      RSP
249
             AE 10
250
                                              #BINCT CLEAR ALL OF THE VARIABLES BETWEEN
      0082
                                      LDX
251
      0084
            7F
                              CLRIT
                                      CLR
                                              , X
                                                      'BINCT' AND 'TIMCT' (INCLUSIVE).NOTE
                                                      THAT THIS SETS THE COUNTER AND THE POS-
252
      0085
            5C
                                      INCX
            A3 22
                                              #TIMCT ITION TO ZERO. THIS MEANS THAT ROTATION
253
      0086
                                      CPX
254
      0088
             23 FA
                                              CLRIT
                                                      SHOULD START IN AN INCREASING (CW)
                                      RIS
                              ***
255
                                                      DIRECTION FROM THE MOST CCW POSITION
                              ***
256
                                                      AFTER A RESET.
                              ***
257
258
      008A
                                                      BACK TO ABSOLUTE ADDRESSING.
                                      ABSOLUTE
                              ***
259
```

```
______
260
261
                         ***
262
                         ***
                                                ESTABLISH I/O PORTS.
263
                         ***
264
     008A
           A6 FF
                                LDA
                                       #-1
                                                PORTS A,B,C ARE CONFIGURED AS
                                                ALL OUTPUT. PORT D IS ALL INPUT
     008C
                                       PORTA+DDR
265
           B7 04
                                STA
                                      PORTB+DDR
                                                 SO THERE IS NO MASK TO SET.
266
     008E
           B7 05
                                STA
                                       PORTC+DDR
267
     0090
           B7 06
                                STA
                         ***
268
                         269
                         ***
270
                                           SET UP THE STATUS REGISTER.
                         ***
271
                                      #%00001000
272
     0092
           A6 08
                                LDA
                                                   |--> SET UP 'L_SET' BIT OF 'STAT'.
                                AND
                                      PORTD
273
           B4 03
     0094
274
     0096
           B7 20
                                STA
                                       STAT
                         ---
275
                                      MOD 32, STAT 0 IS MODULO 32.
276
     0098
           1C 20
                                BSET
277
                         **
                         *********************************
278
279
                         ***
                         ***
                                            INITIALIZE HYSTCT.
280
281
                         ***
     009A
                                LDA
                                      #06
282
          A6 06
          B7 1E
B7 1C
283
     009C
                                STA
                                       HYST
284
     009E
                                STA
                                      HYSTPT
                         ***
285
286
                         **
287
                         **
288
                                 SET UP THE TIMER FOR A 4 MHZ CRYSTAL / 4 = 1 MHZ CLOCK.
                         ***
289
290
                         ***
                               NOTE: THE MASK OPTION REGISTER IS IN ROM. IT IS SET UP AT
291
                         ***
                                     THE END OF THE PROGRAM.
292
                         ***
                         293
294
                         ***
295
           A6 47
     00A0
                                LDA
                                        #BIT6+BIT2+BIT1+BIT0
296
                         ***
                                       (TIM) | (PS2)(PS1)(PS0)
297
                         ***(DISABLE INTERRUPT) (PRESCALE BY 128)
298
                         ***
299
     00A2
           B7 09
                                      TCR
                                STA
                         ***
300
                         ***
301
302
                         *** SET UP THE TIMER.
303
304
     00A4
           A6 FF
                                LDA
                                      #255
                                             1 \text{ MHZ}/(128*255) = 30.6 \text{ (APPROX. 31)}
305
     00A6
           R7 08
                                STA TIMER
306
307
                         308
                         ***
                                             PROVIDES FOR 1 SEC. BLINK INTERVAL.
309
     8A00
           A6 1F
                                LDA
310
     DOAA
           B7 22
                                STA
                                      TIMCT
                                             FOR 2 SEC. INTERVAL JUST USE TIMECT=62, etc.
                         ***
311
                         ***
312
                         ********************
313
314
                         **
315
                         **
                                           SET UP MISCELLANEOUS REGISTER.
316
                         **
317
     OOAC
           1D OA
                               BCLR
                                      B6,MR
                                             ENABLES THE SECOND INTERRUPT.
318
                         **
319
                         ***
                               ***********
320
                         **
321
                                          COUNT = 0 IS DISPLAYED INITIALLY.
322
323
     OOAE
           CD 02 D8
                                JSR
                                      OUTCT
324
     00B1
           10 01
                                      POSTIV, PORTB
                                BSET
325
```

```
326
                              ++
327
      00B3
             9A
                                      CLI
                                                      CLEAR THE INTERRUPT MASK TO GET STARTED.
328
329
      00B4
                                      RELATIVE
                                                      RELATIVE ADDRESSING MUST BE USED FOR THE
                              ***
                                                      REMAINDER OF THE PROGRAM.
330
                              ***
331
                                     332
                              *****
333
                              ** WAIT LOOP. EXECUTES, UNTIL AN INTERRUPT OCCURS.
334
335
336
      00B4
             09 03 0B
                              PAUSE
                                      BRCLR
                                              FUNCT, PORTD, CHHYST WANT TO CHANGE HYST?
                                                                 YES ... GO TO CHHYST.
                              **
337
                                                                 NO ... 'SET, PORTD' SET?
338
      00B7
             06 03 04
                                      BRSET
                                              SET, PORTD, SBIT
             17 20
                                      BCLR
                                              L_SET, STAT
                                                                      NO...CLEAR 'L_SET, STAT'
339
      00BA
      OOBC
             20 F6
                                      BRA
                                              PAUSE
                                                                        AND LOOP.
340
                                                                      YES ... SET 'L_SET, STAT'
341
      OOBE
             16 20
                                      RSET
                                              L_SET, STAT
                              SBIT
342
      0000
             20 F2
                                      BRA
                                              PAUSE
                                                                        AND LOOP.
343
                              344
345
                              **
346
                              ** HYSTERESIS MODIFICATION ROUTINE. PERMITS MODIFICATION OF THE
347
                              ** HYSTERESIS BUFFER WITHOUT REPROGRAMMING.
348
                                                                 YES...
349
                                                                 DISABLE TIMER INTERRUPT.
      00C2
             A6 40
                              CHHYST
                                      LDA
                                              #BIT6
            B7 09
     00C4
350
                                      STA
                                              TCR
351
      0006
                                              #%00001000
352
             A6 08
                                      LDA
                                                                 SAVE 'L_SET'
353
      00C8
             B4 20
                                      AND
                                              STAT
                                                                 INTO
354
      00CA
             B7 21
                                      STA
                                              LSTAT
                                                                  'LSTAT'.
355
      00CC
             A6 08
                                      LDA
                                              #%00001000
                                                                 'SET, PORTD' --> ACCUMULATOR
      00CE
             B4 03
                                      AND
                                              PORTD
356
      0000
                                      CMP
                                                                 HAS THE SET SWITCH BEEN CHANGED?
357
             B1 21
                                              LSTAT
358
     0002
             27 15
                                      BEQ
                                              DISPLA
359
                                                                 YES...
360
      0004
             A6 08
                                      LDA
                                              #%00001000
361
      0006
             B8 20
                                      EOR
                                              STAT
                                                                   |-->CHANGE 'L_SET, STAT',
      8000
             B7 20
362
                                      STA
                                              STAT
             3C 1E
363
      000A
                                      INC
                                              HYST
                                                                 THEN INCREMENT THE HYSTERESIS
364
     0000
             3C 1C
                                      INC
                                              HYSTPT
                                                                 POINTER AND 'HYST' ...
365
366
      000E
             B6 1C
                                      LDA
                                              HYSTPT
             A1 19
367
      00E0
                                      CMP
                                              #25
             23 05
368
      00E2
                                      BLS
                                              DISPLA
                                                                      -- BUT NOT ABOVE 25.
369
370
      00E4
                                                                             THEN--->
             4F
                                      CLRA
             B7 1E
371
      00E5
                                      STA
                                              HYST
             B7 1C
372
      00E7
                                      STA
                                              HYSTPT
                              ***
373
                                                                 NO... JUST---->
                                              #%00000000
374
      00E9
             A6 00
                              DISPLA
                                      LDA
375
      00EB
             B7 00
                                              PORTA
                                      STA
                                              #%11000000
376
      00ED
                                      LDA
             A6 C0
     00EF
             B7 01
                                              PORTB
377
                                      STA
378
                                                                       -- DISPLAY CURRENT 'HYST'.
379
      00F1
             BE 1C
                                      LDX
                                              HYSTPT
380
      00F3
             D6 03 28
                                      LDA
                                              TABLE,X
381
      00F6
             B7 02
                                      STA
                                              PORTC
382
                                                                 IS 'HYST' SETTING COMPLETE?
                                              FUNCT, PORTD, CHHYST NO... KEEP CHECKING 'SET'.
383
      00F8
             09 03 C7
                                      BRCLR
384
      00FB
             04 20 04
                                      BRSET
                                              NEGTIV, STAT, SIGN
                                                                 YES ... RESET THE DISPLAY.
             1C 01
                                              POSTIV, PORTB
385
      00FE
                                      BSET
386
      0100
             20 02
                                      BRA
387
      0102
             1D 01
                              SIGN
                                      BCLR
                                              POSTIV, PORTB
388
     0104
                                      BRSET
                                              POSCT, STAT, SHOPOS
             08 20 05
                              DIR
389
390
      0107
             CD 02 D8
                                      JSR
                                              OUTCT
391
      010A
             20 03
                                      BRA
                                              DUNCHG
```

```
392
                              ***
393
      010C
             CD 02 E5
                              SHOPOS
                                     JSR
                                             OUTPOS
394
                                              FLASH STAT NO INT IF THE DISPLAY IS TO BLINK ...
395
      010F
             OB 20 04
                              DUNCHG
                                     BRCLR
             A6 07
                                                                ENABLE TIMER INTERRUPT AND RESET
396
      0112
                                      LDA
                                              #BIT2+BIT1+BIT0
      0114
             B7 09
                                                                TIMER PRESCALER
397
                                      STA
                                              TCR
                                                                PRIOR TO RETURNING.
398
      0116
             20 9C
                              NO INT
                                     BRA
                                             PAUSE
                              ++=
399
                              **
400
                              ********************************
401
                              ** MAXIMUM EXECUTION TIME FOR THE REMAINDER OF THE PROGRAM OCCURS
402
403
                              ** IF THE COUNTER ROTATES THROUGH ZERO AS THE DISPLAY MODE IS CHANGED
404
                                FROM THE BLINKING MODE TO THE COUNT MODE AT THE SAME TIME THAT THE
405
                              ** BLINKING ROUTINE IS CAUSING THE DISPLAY TO TOGGLE TO SHOW THE
                              ** POSITION IN DEGREES.
406
407
                              **
                                     MAXIMUM EXECUTION TIME = 67 + 140 + 618 = 825 CLOCK CYCLES.
                              **
408
                              **************************************
409
                              **
410
411
                              **MODE CHANGE ROUTINE. CHANGES THE DISPLAY MODE FROM
                              **
                                      COUNT -> POSITION -> BLINKING -> COUNT ->....(ETC.)
412
                              **
413
                                      MAXIMUM EXECUTION TIME OF 127 CLOCK CYCLES OCCURS WHEN THE
                              **
                                      DISPLAY MODE IS CHANGED FROM DISPLAYING THE COUNT TO DISPLAYING
414
                              **
415
                                      THE POSITION (IN DEGREES).
                              **
                                      IF THE DISPLAY IS CHANGED FROM BLINKING TO A COUNT DISPLAY
416
                              **
                                      EXECUTION TIME IS 67 CLOCK CYCLES.
417
                              **
418
419
      0118
             1F OA
                              CHMODE BCLR
                                             B7,MR
                                                                AVOID REPEATED INTERRUPTS.
420
                              **
421
      011A
             OA 20 10
                                             FLASH, STAT, DIS_CT IF FLASHING, DISPLAY COUNT...
                                     RRSET
             09 20 07
                                             POSCT, STAT, DISPOS IF SHOWING COUNT, DISPLAY POSITION...
422
      011D
                                     BRCLR
             1A 20
423
      0120
                                     BSET
                                             FLASH, STAT
                                                                ELSE, BLINK.
424
425
      0122
            A6 07
                                     LDA
                                                                ENABLE TIMER INTERRUPT AND RESET
                                              #BIT2+BIT1+BIT0
426
      0124
             B7 09
                                     STA
                                                                TIMER PRESCALER.
                                             TCR
427
      0126
            80
                                     RTI
428
                              **
429
      0127
             18 20
                             DISPOS
                                     BSET
                                              POSCT, STAT
430
      0129
             CD 02 E5
                                                                |-- DISPLAY CURRENT POSITION, AND WAIT.
                                      JSR
                                              OUTPOS
431
     012C
             80
                                     RTI
432
            A6 47
433
     0120
                                     LDA
                                             #BIT6+BIT2+BIT1+BIT0 DISABLE TIMER INTERRUPT AND RESET
                             DIS_CT
434
     012F
            B7 09
                                     STA
                                             TCR
                                                                    TIMER PRESCALER.
435
             19 20
      0131
                                     BCLR
                                             POSCT, STAT
436
      0133
             1B 20
                                     BCLR
                                             FLASH, STAT
437
                                                                  - DISPLAY CURRENT COUNT, AND WAIT.
438
      0135
             CD 02 D8
                                      JSR
                                              OUTCT
439
     0138
             80
                                     RTI
440
441
                                     ********
442
443
                              ** BLINK ROUTINE. INTERRUPT ROUTINE TO CHANGE THE DISPLAY FROM POSITION
444
                              **
                                      TO COUNT OR VICE VERSA EVERY 31 ST TIMER INTERRUPT IF THE
445
                              **
                                       'FLASH' BIT OF 'STAT' IS SET.
446
                              ++
                                      MAXIMUM EXECUTION TIME OF 140 CLOCK CYCLES OCCURS WHEN THE
447
                              **
                                      DISPLAY IS TOGGLED FROM A COUNT DISPLAY TO A POSITION DISPLAY.
                              **
448
449
             0139
                              BLINK
                                     EQU
450
      0139
             OF 09 DC
                                     BRCLR
                                                                    IF THE INTERRUPT WAS NOT A TIMER
                                             TIR, TCR, CHMODE
451
                                                                    INTERRUPT IT MUST BE FROM INT2.
452
                              **
453
      013C
             1F 09
                                     BCLR
                                             TIR, TCR
                                                                   AVOID REPEATED TIMER INTERRUPTS.
454
                              **
455
      013E
             3A 22
                                     DEC
                                              TIMCT
                                                                    IF THERE HAVE BEEN 31 TIMER
456
      0140
             27 01
                                      BEQ
                                              CHGDIS
                                                                    INTERRUPTS (1 SEC), IT'S TIME TO
457
```

CHANGE THE DISPLAY.

```
458
      0142
             80
                                      RTI
                                                                    OTHERWISE, IT'S BACK TO WORK.
459
             A6 1F
      0143
460
                              CHGDIS
                                      LDA
                                              #31
                                                                    RESET TIMET TO 31 (1 SEC. INTERVAL).
      0145
             B7 22
461
                                              TIMCT
                                      STA
462
      0147
463
             B6 20
                                      LDA
                                              STAT
                                                                I -- CHANGE 'POSCT' BIT OF 'STAT'.
464
      0149
             A8 10
                                              #%00010000
                                      EOR
465
      014B
             B7 20
                                      STA
                                              STAT
466
                              **
467
      0140
             08 20 04
                                      BRSET
                                              POSCT, STAT, POSCUT
                                                                    DECIDE ON CORRECT DISPLAY.
468
469
                              *******
                                            CHANGE THE DISPLAY TO SHOW THE COUNT .... ************
470
                              **
471
      0150
             CD 02 D8
                                      JSR
                                              OUTCT
                                      RTI
472
      0153
             80
473
                              ******
                                            OR HAVE THE DISPLAY SHOW THE POSITION. ************
474
475
                              ++
476
      0154
             CD 02 E5
                              POSOUT JSR
                                              OUTPOS
477
      0157
             80
                                      RTI
478
                              ***************
479
480
                              **
                              **
                                                         COUNT ROUTINE.
481
                              **
                                        WHEN A COUNT IS RECEIVED THIS IS THE ENTRY POINT .
482
                              **
483
                                        MAXIMUM EXECUTION TIME OF 618 CLOCK CYCLES OCCURS WHEN THE
484
                                        COUNTER ROTATES CCW THROUGH ZERO AND THE POSITION (IN DEGREES)
485
                                        IS BEING DISPLAYED.
                              **
486
487
                              **
                              ** CURRENT DIRECTION OF ROTATION IS DETERMINED BY INSPECTING THE STATUS
488
                              ** OF 'CH_A' AND 'CH_B'. THE FOUR POSSIBILITIES AND THE ASSOCIATED
489
490
                              ** DIRECTION OF ROTATION ARE AS SHOWN BELOW. NOTE THAT THIS SCHEME
                                 PREVENTS MULTIPLE OSCILLATIONS ABOUT A SINGLE POINT FROM
491
                                 REPEATEDLY INCREMENTING OR DECREMENTING THE COUNTER.
492
                              **
493
                              **
494
                              **
495
                                      CH A
                                                CH B
                                                          DIRECTION
                                                                            COUNT THE PULSE?
496
                                                         OF ROTATION
497
498
                              **
                                                                                  NO
                                       LO
                                                 LO
                                                             CW
499
                              **
                                       LO
                                                 ΗI
                                                             CCW
                                                                                  YES
500
                              **
                                       ΗI
                                                 LO
                                                             CCW
                                                                                  NO
                              **
501
                                       ΗI
                                                 HΙ
                                                             CW
                                                                                   YES
502
                              **
503
504
                              *****
                                        FIRST SEE IF WE ARE SUPPOSED TO COUNT THIS INTERUPT.
                                                                                             ******
                              **
505
506
             0158
                              COUNT
                                      EQU
                                              CH B, PORTD, OKCT IF CH B IS LO WE DON'T COUNT THE
507
      0158
             OA 03 01
                                      BRSET
508
     015B
             80
                                      RTI
                                                                 INTERRUPT.
509
510
                                              IF THE INTERRUPT IS VALID UPDATE 'STAT'. ***********
                              **
511
512
      015C
             A6 7F
                                      LDA
                                              #%01111111
                              OKCT
513
      015E
             B4 20
                                      AND
                                              STAT
                                                              SAVE ALL OF THE OLD 'STAT' EXCEPT THE
             B7 20
      0160
                                                              DIRECTION OF ROTATION.
514
                                      STA
                                              STAT
             A6 80
      0162
                                              #%10000000
515
                                      LDA
516
      0164
             B4 03
                                                              'CH A, PORTD' INDICATES THE DIRECTION
                                      AND
                                              PORTD
517
                                                              OF ROTATION AND BECOMES 'UD, STAT'.
      0166
                                                              ADD THE RESULTS TO GET
518
             BA 20
                                      ORA
                                              STAT
519
      0168
             B7 20
                                      STA
                                              STAT
                                                              THE NEW 'STAT'.
520
521
                              ** DECIDE IF THE "SLACK" DUE TO BACKLASH/HYSTERESIS HAS BEEN TAKEN OUT.
522
523
      016A
             OE 20 09
                                      BRSET
                                              UD, STAT, HYSTCK IF ROTATING CW SEE BELOW.
```

524	0160	B6 1F		LDA	HYSTCT	ELSE, SEE IF WE DECREMENT THIS TIME.
525	016F	27 4B		BEQ	CCM	IF HYSTCT=0, GO TO THE COUNT DOWN
526	• • • • • • • • • • • • • • • • • • • •		**			ROUTINE.
527	0171	40.04		SUB	#1	ELSE, DECREMENT THE HYSTERESIS COUNTER,
		A0 01				ELSE, DECKEMENT THE HTSTERESTS COUNTER,
528	0173	B7 1F		STA	HYSTCT	
529	0175	80		RTI		AND WAIT FOR THE NEXT INTERRUPT.
530			食物			
531	0176	B6 1E	HYSTCK	LDA	HYST	IF ROTATING CW
532	0178	B1 1F		CMP	HYSTCT	AND HYST = HYSTCT
533	017A	27 03		BEQ	CW	COUNT THE PULSE .
534	017C	3C 1F		INC	HYSTCT	ELSE, INCREMENT THE HYSTERESIS COUNTER,
535	017E	80		RTI		AND WAIT FOR ANOTHER PULSE.
536			**			
537			**			
538			*****	*****	******	***********
539			**			
540			**		CLC	OCKWISE ROUTINE.
541			**			
		0476	CW	EQU	s	
542		017F	t#	EUU	•	
543						
544			***			
545			****	*****	INCREMENT THE	BINARY COUNTER (BINCT). ************
546			***			
547	017F	B6 11		LDA	LOBIN BEGIN	AT THE LSB OF THE BINARY COUNTER.
548	0181	AB 01		ADD		I = LOBIN + 1 ; CARRY -> C,CCR
549	0183	B7 11		STA	LOBIN	- LOUIN . I , GARRI > C, CCR
	0103	87 11	***	SIA	LODIN	
550			***			
551	0185	B6 10		LDA	HIBIN	
552	0187	A9 00		ADC	#0	ADD THE CARRY TO THE HIGH BYTE.
553	0189	B7 10		STA	HIBIN	
554			***			
555			***			
556			*****	******	*** CID/SET N	400_32 APPROPRIATELY. *************
557			***		CER/SET P	NO_JE APPROPRIATELT.
	0400	T/ 44				
558	018B	B6 11		LDA	LOBIN	IF THE LOW FIVE BITS OF 'LOBIN' ARE NOT
559	018D	A4 1F		AND	#%00011111	NOT THEN THE NUMBER ISN'T A MODULO 32 NUMBER.
560	018F	26 04		BNE	NOT_32	
561			***			
					70	
562	0191	1C 20		BSET	MOD 32.STAT	
					MOD_32,STAT	
563	0191 0193	1C 20 20 02	***	BSET	DIRCHK	
563 564	0193	20 02		BRA	DIRCHK	
563 564 565			NOT_32	BRA		
563 564 565 566	0193	20 02	NOT_32	BRA	DIRCHK	
563 564 565 566 567	0193 0195	20 02 1D 20	NOT_32	BRA	DIRCHK	
563 564 565 566	0193	20 02	NOT_32	BRA BCLR	DIRCHK	
563 564 565 566 567	0193 0195	20 02 1D 20	NOT_32	BRA BCLR	DIRCHK MOD_32,STAT	IF HIBIN < 0 , WE'RE ROTATING CW TOWARD
563 564 565 566 567 568	0193 0195 0197	20 02 1D 20 B6 10	NOT_32	BRA BCLR LDA	DIRCHK MOD_32,STAT HIBIN	· · · · · · · · · · · · · · · · · · ·
563 564 565 566 567 568 569 570	0193 0195 0197	20 02 1D 20 B6 10	NOT_32 *** *** DIRCHK	BRA BCLR LDA	DIRCHK MOD_32,STAT HIBIN	IF HIBIN < 0 , WE'RE ROTATING CW TOWARD THE ORIGIN.
563 564 565 566 567 568 569 570 571	0193 0195 0197 0199	20 02 1D 20 B6 10 2B 19	NOT_32 *** *** DIRCHK	BRA BCLR LDA BMI	DIRCHK MOD_32,STAT HIBIN CWNEG	THE ORIGIN.
563 564 565 566 567 568 569 570 571 572	0193 0195 0197 0199 0198	20 02 1D 20 B6 10 2B 19 26 10	NOT_32 *** *** DIRCHK	BRA BCLR LDA BMI BNE	DIRCHK MOD_32,STAT HIBIN CWNEG CWPOS	THE ORIGIN. ELSE IF BINCT .NE. 0 ,
563 564 565 566 567 568 569 570 571 572 573	0193 0195 0197 0199 0198 0190	20 02 1D 20 B6 10 2B 19 26 10 B6 11	NOT_32 *** *** DIRCHK	BRA BCLR LDA BMI BNE LDA	DIRCHK MOD_32,STAT HIBIN CWNEG CWPOS LOBIN	THE ORIGIN. ELSE IF BINCT .NE. 0 , WE'RE ROTATING CW
563 564 565 566 567 568 569 570 571 572 573 574	0193 0195 0197 0199 0198	20 02 1D 20 B6 10 2B 19 26 10	NOT_32 *** *** DIRCHK ***	BRA BCLR LDA BMI BNE	DIRCHK MOD_32,STAT HIBIN CWNEG CWPOS	THE ORIGIN. ELSE IF BINCT .NE. 0 ,
563 564 565 566 567 568 569 570 571 572 573	0193 0195 0197 0199 0198 0190	20 02 1D 20 B6 10 2B 19 26 10 B6 11	NOT_32 *** *** DIRCHK	BRA BCLR LDA BMI BNE LDA	DIRCHK MOD_32,STAT HIBIN CWNEG CWPOS LOBIN	THE ORIGIN. ELSE IF BINCT .NE. 0 , WE'RE ROTATING CW
563 564 565 566 567 568 569 570 571 572 573 574	0193 0195 0197 0199 0198 0190	20 02 1D 20 B6 10 2B 19 26 10 B6 11	NOT_32 *** *** DIRCHK ***	BRA BCLR LDA BMI BNE LDA	DIRCHK MOD_32,STAT HIBIN CWNEG CWPOS LOBIN	THE ORIGIN. ELSE IF BINCT .NE. 0 , WE'RE ROTATING CW AWAY FROM THE ORIGIN.
563 564 565 566 567 568 569 570 571 572 573 574 575 576	0193 0195 0197 0199 0198 0190 019F	20 02 1D 20 B6 10 2B 19 26 10 B6 11 26 0C	NOT_32 *** *** DIRCHK ***	BRA BCLR LDA BMI BNE LDA BNE	DIRCHK MOD_32,STAT HIBIN CWNEG CWPOS LOBIN CWPOS	THE ORIGIN. ELSE IF BINCT .NE. 0 , WE'RE ROTATING CW AWAY FROM THE ORIGIN. ELSE, WE'VE GONE THROUGH ORIGIN IN CW
563 564 565 566 567 568 569 570 571 572 573 574 575 576 577	0193 0195 0197 0199 0198 0190 019F	20 02 1D 20 B6 10 2B 19 26 10 B6 11 26 0c 15 20	NOT_32 *** DIRCHK *** ***	BRA BCLR LDA BMI BNE LDA BNE BCLR	DIRCHK MOD_32,STAT HIBIN CWNEG CWPOS LOBIN CWPOS NEGTIV,STAT	THE ORIGIN. ELSE IF BINCT .NE. 0 , WE'RE ROTATING CW AWAY FROM THE ORIGIN.
563 564 565 566 567 568 569 570 571 572 573 574 575 576 577 578	0193 0195 0197 0199 0198 0190 019F 01A1	20 02 1D 20 B6 10 2B 19 26 10 B6 11 26 0c 15 20 AE 12	NOT_32 *** DIRCHK *** ***	BRA BCLR LDA BMI BNE LDA BNE BCLR LDX	DIRCHK MOD_32,STAT HIBIN CWNEG CWPOS LOBIN CWPOS NEGTIV,STAT #PTR3	THE ORIGIN. ELSE IF BINCT .NE. 0 , WE'RE ROTATING CW AWAY FROM THE ORIGIN. ELSE, WE'VE GONE THROUGH ORIGIN IN CW
563 564 565 566 567 568 569 570 571 572 573 574 575 576 577 578 579	0193 0195 0197 0199 0198 0190 019F 01A1 01A3 01A5	20 02 1D 20 B6 10 2B 19 26 10 B6 11 26 0c 15 20 AE 12 7F	NOT_32 *** DIRCHK *** ***	BRA BCLR LDA BMI BNE LDA BNE BCLR LDX CLR	DIRCHK MOD_32,STAT HIBIN CWNEG CWPOS LOBIN CWPOS NEGTIV,STAT #PTR3 ,X	THE ORIGIN. ELSE IF BINCT .NE. 0 , WE'RE ROTATING CW AWAY FROM THE ORIGIN. ELSE, WE'VE GONE THROUGH ORIGIN IN CW DIRECTION. CLR NEGATIVE SIGN.
563 564 565 566 567 568 569 570 571 572 573 574 575 576 577 578 579 580	0193 0195 0197 0199 0198 0190 019F 01A1 01A3 01A5 01A6	20 02 1D 20 B6 10 2B 19 26 10 B6 11 26 0C 15 20 AE 12 7F 5C	NOT_32 *** DIRCHK *** ***	BRA BCLR LDA BMI BNE LDA BNE BCLR LDX CLR INCX	DIRCHK MOD_32,STAT HIBIN CWNEG CWPOS LOBIN CWPOS NEGTIV,STAT #PTR3 ,X	THE ORIGIN. ELSE IF BINCT .NE. 0 , WE'RE ROTATING CW AWAY FROM THE ORIGIN. ELSE, WE'VE GONE THROUGH ORIGIN IN CW
563 564 565 566 567 568 569 570 571 572 573 574 575 576 577 578 579 580 581	0193 0195 0197 0199 0198 0190 019F 01A1 01A3 01A5 01A6 01A7	20 02 1D 20 B6 10 2B 19 26 10 B6 11 26 0c 15 20 AE 12 7F 5C A3 19	NOT_32 *** DIRCHK *** ***	BRA BCLR LDA BMI BNE LDA BNE LDA CLR INCX CPX	DIRCHK MOD_32,STAT HIBIN CWNEG CWPOS LOBIN CWPOS NEGTIV,STAT #PTR3 ,X	THE ORIGIN. ELSE IF BINCT .NE. 0 , WE'RE ROTATING CW AWAY FROM THE ORIGIN. ELSE, WE'VE GONE THROUGH ORIGIN IN CW DIRECTION. CLR NEGATIVE SIGN.
563 564 565 566 567 568 569 570 571 572 573 574 575 576 577 578 579 580 581 582	0193 0195 0197 0199 0198 0190 019F 01A1 01A3 01A5 01A6	20 02 1D 20 B6 10 2B 19 26 10 B6 11 26 0c 15 20 AE 12 7F 5C A3 19 23 FA	NOT_32 *** DIRCHK *** ***	BRA BCLR LDA BMI BNE LDA BNE BCLR LDX CLR INCX	DIRCHK MOD_32,STAT HIBIN CWNEG CWPOS LOBIN CWPOS NEGTIV,STAT #PTR3 ,X	THE ORIGIN. ELSE IF BINCT .NE. 0 , WE'RE ROTATING CW AWAY FROM THE ORIGIN. ELSE, WE'VE GONE THROUGH ORIGIN IN CW DIRECTION. CLR NEGATIVE SIGN.
563 564 565 566 567 568 569 570 571 572 573 574 575 576 577 578 579 580 581	0193 0195 0197 0199 0198 0190 019F 01A1 01A3 01A5 01A6 01A7	20 02 1D 20 B6 10 2B 19 26 10 B6 11 26 0c 15 20 AE 12 7F 5C A3 19	NOT_32 *** DIRCHK *** ***	BRA BCLR LDA BMI BNE LDA BNE LDA CLR INCX CPX	DIRCHK MOD_32,STAT HIBIN CWNEG CWPOS LOBIN CWPOS NEGTIV,STAT #PTR3 ,X #THOUTH	THE ORIGIN. ELSE IF BINCT .NE. 0 , WE'RE ROTATING CW AWAY FROM THE ORIGIN. ELSE, WE'VE GONE THROUGH ORIGIN IN CW DIRECTION. CLR NEGATIVE SIGN.
563 564 565 566 567 568 569 570 571 572 573 574 575 576 577 578 579 580 581 582	0193 0195 0197 0199 0198 0190 019F 01A1 01A3 01A5 01A6 01A7 01A9	20 02 1D 20 B6 10 2B 19 26 10 B6 11 26 0c 15 20 AE 12 7F 5C A3 19 23 FA	NOT_32 *** DIRCHK *** ***	BRA BCLR LDA BMI BNE LDA BNE LDA CLR INCX CPX BLS	DIRCHK MOD_32,STAT HIBIN CWNEG CWPOS LOBIN CWPOS NEGTIV,STAT #PTR3 ,X #THOUTH CLRIT2	THE ORIGIN. ELSE IF BINCT .NE. 0 , WE'RE ROTATING CW AWAY FROM THE ORIGIN. ELSE, WE'VE GONE THROUGH ORIGIN IN CW DIRECTION. CLR NEGATIVE SIGN. RESET ALL COUNTERS AND DEGRES TO ZERO.
563 564 565 566 567 568 569 570 571 572 573 574 575 576 577 578 579 580 581 582 583 584	0193 0195 0197 0199 0198 0190 019F 01A1 01A3 01A5 01A6 01A7 01A9 01AB	20 02 1D 20 B6 10 2B 19 26 10 B6 11 26 0c 15 20 AE 12 7F 5C A3 19 23 FA 20 4C	NOT_32 *** *** DIRCHK *** *** CLRIT2	BRA BCLR LDA BMI BNE LDA BNE LDA CLR INCX CPX BLS BRA	DIRCHK MOD_32,STAT HIBIN CWNEG CWPOS LOBIN CWPOS NEGTIV,STAT #PTR3 ,X #THOUTH CLRIT2 UPOUT	THE ORIGIN. ELSE IF BINCT .NE. 0 , WE'RE ROTATING CW AWAY FROM THE ORIGIN. ELSE, WE'VE GONE THROUGH ORIGIN IN CW DIRECTION. CLR NEGATIVE SIGN. RESET ALL COUNTERS AND DEGRES TO ZERO.
563 564 565 566 567 568 569 570 571 572 573 574 575 576 577 578 579 580 581 582 583 584 585	0193 0195 0197 0199 0198 0190 019F 01A1 01A3 01A5 01A6 01A7 01A9 01AB	20 02 1D 20 B6 10 2B 19 26 10 B6 11 26 0C 15 20 AE 12 7F 5C A3 19 23 FA 20 4C AD 5E	NOT_32 *** *** DIRCHK *** *** CLRIT2	BRA BCLR LDA BMI BNE LDA BNE LDA CLR INCX CPX BLS BRA BSR	DIRCHK MOD_32,STAT HIBIN CWNEG CWPOS LOBIN CWPOS NEGTIV,STAT #PTR3 ,X #THOUTH CURIT2 UPOUT ADDBCD	THE ORIGIN. ELSE IF BINCT .NE. 0 , WE'RE ROTATING CW AWAY FROM THE ORIGIN. ELSE, WE'VE GONE THROUGH ORIGIN IN CW DIRECTION. CLR NEGATIVE SIGN. RESET ALL COUNTERS AND DEGRES TO ZERO.
563 564 565 566 567 568 569 570 571 572 573 574 575 576 577 578 579 580 581 582 583 584 585 586	0193 0195 0197 0199 0198 0190 019F 01A1 01A3 01A5 01A6 01A7 01A9 01AB	20 02 1D 20 B6 10 2B 19 26 10 B6 11 26 0C 15 20 AE 12 7F 5C A3 19 23 FA 20 4C AD 5E CD 02 32	NOT_32 *** *** DIRCHK *** *** CLRIT2	BRA BCLR LDA BMI BNE LDA BNE LDA CLR INCX CPX BLS BRA BSR JSR	DIRCHK MOD_32,STAT HIBIN CWNEG CWPOS LOBIN CWPOS NEGTIV,STAT #PTR3 ,X #THOUTH CLRIT2 UPOUT ADDBCD INCPOS	THE ORIGIN. ELSE IF BINCT .NE. 0 , WE'RE ROTATING CW AWAY FROM THE ORIGIN. ELSE, WE'VE GONE THROUGH ORIGIN IN CW DIRECTION. CLR NEGATIVE SIGN. RESET ALL COUNTERS AND DEGRES TO ZERO.
563 564 565 566 567 568 569 570 571 572 573 574 575 576 577 578 579 580 581 582 583 584 585 586 587	0193 0195 0197 0199 0198 0190 019F 01A1 01A3 01A5 01A6 01A7 01A9 01AB	20 02 1D 20 B6 10 2B 19 26 10 B6 11 26 0C 15 20 AE 12 7F 5C A3 19 23 FA 20 4C AD 5E	NOT_32 *** DIRCHK *** *** CLRIT2 *** CWPOS	BRA BCLR LDA BMI BNE LDA BNE LDA CLR INCX CPX BLS BRA BSR	DIRCHK MOD_32,STAT HIBIN CWNEG CWPOS LOBIN CWPOS NEGTIV,STAT #PTR3 ,X #THOUTH CURIT2 UPOUT ADDBCD	THE ORIGIN. ELSE IF BINCT .NE. 0 , WE'RE ROTATING CW AWAY FROM THE ORIGIN. ELSE, WE'VE GONE THROUGH ORIGIN IN CW DIRECTION. CLR NEGATIVE SIGN. RESET ALL COUNTERS AND DEGRES TO ZERO.
563 564 565 566 567 568 569 570 571 572 573 574 575 576 577 578 579 580 581 582 583 584 585 586 587 588	0193 0195 0197 0199 0198 0190 019F 01A1 01A3 01A5 01A6 01A7 01A9 01AB	20 02 1D 20 B6 10 2B 19 26 10 B6 11 26 0C 15 20 AE 12 7F 5C A3 19 23 FA 20 4C AD 5E CD 02 32 20 45	NOT_32 *** DIRCHK *** *** CLRIT2 *** CWPOS ***	BRA BCLR LDA BMI BNE LDA BNE LDA CLR INCX CPX BLS BRA BSR JSR BRA	DIRCHK MOD_32,STAT HIBIN CWNEG CWPOS LOBIN CWPOS NEGTIV,STAT #PTR3 ,X #THOUTH CLRIT2 UPOUT ADDBCD INCPOS	THE ORIGIN. ELSE IF BINCT .NE. 0 , WE'RE ROTATING CW AWAY FROM THE ORIGIN. ELSE, WE'VE GONE THROUGH ORIGIN IN CW DIRECTION. CLR NEGATIVE SIGN. RESET ALL COUNTERS AND DEGRES TO ZERO.
563 564 565 566 567 568 569 570 571 572 573 574 575 576 577 578 579 580 581 582 583 584 585 586 587	0193 0195 0197 0199 0198 0190 019F 01A1 01A3 01A5 01A6 01A7 01A9 01AB	20 02 1D 20 B6 10 2B 19 26 10 B6 11 26 0C 15 20 AE 12 7F 5C A3 19 23 FA 20 4C AD 5E CD 02 32	NOT_32 *** DIRCHK *** *** CLRIT2 *** CWPOS	BRA BCLR LDA BMI BNE LDA BNE LDA CLR INCX CPX BLS BRA BSR JSR	DIRCHK MOD_32,STAT HIBIN CWNEG CWPOS LOBIN CWPOS NEGTIV,STAT #PTR3 ,X #THOUTH CLRIT2 UPOUT ADDBCD INCPOS	THE ORIGIN. ELSE IF BINCT .NE. 0 , WE'RE ROTATING CW AWAY FROM THE ORIGIN. ELSE, WE'VE GONE THROUGH ORIGIN IN CW DIRECTION. CLR NEGATIVE SIGN. RESET ALL COUNTERS AND DEGRES TO ZERO.

```
590
     01B7
            CD 02 9A
                                            DECPOS
                                    JSR
591
     01BA
            20 30
                                    BRA
                                            UPOLIT
592
                             ***
                             **
593
                             ****
                                   *************
594
                             **
595
                             **
596
                                                 COUNTER-CLOCKWISE ROUTINE.
597
                             **
598
            01BC
                             CCM
                                    EQU
                                            $
599
                             **
                             ***
600
601
                             ***
602
603
     01BC
                                                         IF THE LOW FIVE BITS OF 'LOBIN' ARE NOT
            B6 11
                                    LDA
                                            LORIN
604
     01BE
            A4 1F
                                    AND
                                            #%00011111 ZERO THEN THE NUMBER ISN'T A MODULO 32 NUMBER.
     01C0
605
            26 04
                                            NO_32
                                    BNE
606
607
     01C2
            1C 20
                                    BSET
                                            MOD 32, STAT
608
     01C4
            20 02
                                            DECBIN
                                    BRA
                             ***
609
     01C6
610
            1D 20
                             NO 32
                                    BCLR
                                            MOD 32, STAT
611
                             ***
612
                             ****** DECREMENT THE BINARY COUNTER (BINCT). ***********
613
                             ***
614
615
     0108
            86 11
                             DECBIN
                                    LDA
                                            LOBIN
                                                    BEGIN AT THE LSB OF THE BINARY COUNTER.
     01CA
            A0 01
                                     SHR
                                            #1
                                                    LOBIN = LOBIN - 1 ; BORROW -> C,CCR
616
     01CC
            B7 11
                                    STA
                                            LOBIN
617
618
                             ***
     01CE
            B6 10
                                     LDA
                                            HIBIN
619
620
     0100
            A2 00
                                    SBC
                                            #0
                                                    SUBTRACT THE CARRY FROM THE HIGH BYTE.
            B7 10
621
     0102
                                    STA
                                            HIBIN
622
     0104
            B6 10
                                    LDA
623
                                            HIBIN
624
     0106
            2A 1B
                                    BPL
                                            CCWPOS
                                                         IF HIBIN .GE. 0 , WE'RE ROTATING CCW TOWARD
625
                                                          THE ORIGIN.
626
     01D8
            A1 FF
                                    CMP
                                            #-1
627
     01DA
            26 10
                                    BNE
                                            CCWNEG
                                                    -- ELSE IF BINCT .NE. -1
628
     01DC
            86 11
                                     LDA
                                            LOBIN
                                                       --WE'RE ROTATING CCW AWAY
629
     01DE
            A1 FF
                                    CMP
                                            #-1
                                                     -- FROM THE ORIGIN.
                                            CCWNEG --
630
     01E0
            26 OA
                                    BNE
                                                          ELSE, WE'VE GONE THROUGH ORIGIN IN CCW
631
     01E2
            14 20
                                    BSET
                                            NEGTIV, STAT
                             ***
632
                                                          DIRECTION. SET NEGATIVE SIGN.
                             ***
633
                                                          AND SET ALL COUNTERS APPROPRIATELY.
     01E4
            AE 12
                                    LDX
                                            #PTR3
634
     01E6
635
            7F
                             CLREM
                                     CLR
                                            ,х
     01E7
                                     INCX
                                                        -- RESET ALL COUNTERS AND DEGRES TO ZERO.
636
            5C
637
     01E8
            A3 19
                                    CPX
                                            #THOUTH
638
     01EA
            23 FA
                                     BLS
                                            CLREM
639
                             ***
640
     01EC
            AD 1F
                             CCWNEG
                                    BSR
                                            ADDBCD
641
     01EE
            CD 02 32
                                     JSR
                                            INCPOS
642
     01F1
            20 06
                                     BRA
                                            UPOUT
643
644
     01F3
            CD 02 7A
                             CCWPOS
                                    JSR
                                            SUBBCD
645
     01F6
            CD 02 9A
                                     JSR
                                            DECPOS
646
                             ***
647
648
                             **
649
                             ****
650
                             **
651
                             ** OUTPUT ROUTINE. ROUTINE TO PRINT DATA TO THE OUTPUT PORTS.
                             **
652
                                     CALLING THE APPROPRIATE SUBROUTINE. ('OUTCT' TO OUTPUT THE
                             **
653
                                     THE COUNT AND 'OUTPOS' TO OUTPUT THE POSITION).
654
            01F9
655
                             UPOUT EQU
```

```
656
      01F9
             04 20 04
                                                NEGTIV, STAT, MINUS
657
                                        BRSET
             1C 01
                                                POSTIV, PORTB
658
      01FC
                                        BSET
659
      01FE
             20 02
                                        BRA
                                                DISCHK
660
                                **
                                                                             SET THE NEGATIVE SIGN
661
      0200
             1D 01
                                MINUS
                                        BCLR
                                                POSTIV, PORTB
                                                                             APPROPRIATELY.
                                **
662
663
      0202
             09 20 04
                                        BRCLR
                               DISCHK
                                                POSCT, STAT, PUTCT
664
665
      0205
             CD 02 E5
                                        JSR
                                                OUTPOS
      0208
666
             80
                                        RTI
667
                                **
      0209
668
             CD 02 D8
                                PUTCT
                                        JSR
                                                OUTCT
669
      020C
             80
                                        RTI
670
671
                                ******
                                             SUBROUTINE TO INCREMENT THE BCD COUNTER (BCDCT). ********
672
673
                                ***
      0200
                                ADDBCD LDA
                                                CTPTR1
674
             B6 16
675
      020F
             AB 01
                                        ADD
                                                #1
                                                #99
                                        CMP
                                                         CTPTR > 99 ?
676
      0211
             A1 63
             23 05
                                                         NO, WE'RE OK HERE. LOOK UP THE FIRST TWO DIGITS.
677
      0213
                                        BLS
                                                OK1
678
      0215
             A0 64
                                        SHR
                                                #100
                                                         YES ... MODIFY THE CTPTR,
                                                         SET THE CARRY, AND
679
      0217
             99
                                        SEC
680
      0218
             20 01
                                        BRA
                                                OK1A
                                                         USE TABLE LOOK UP.
                               ***
681
682
      021A
             98
                                OK1
                                        CLC
                                                                NO CARRY EXISTS IF WE ENTER AT THIS POINT.
683
      021B
             B7 16
                               OK1A
                                        STA
                                                CTPTR1 --
684
      021D
             97
                                        TAX
685
                                                             -- LOOK UP THE TWO LEAST SIGNIFICANT DIGITS.
686
      021E
             D6 03 28
                                        LDA
                                                TABLE,X
687
      0221
             B7 1B
                                        STA
                                                TENONE --
688
      0223
             24 OC
                                        BCC
                                                NOMO
                                                               AND CONTINUE ONLY IF THERE WAS A CARRY.
689
                               ***
                               ***
690
      0225
             B6 15
691
                                        LDA
                                                CTPTR2
             A9 00
692
      0227
                                        ADC
                                                #0
                                                         ADD THE CARRY.
693
      0229
             B7 15
                                        STA
                                                CTPTR2 --
694
      022B
             97
                                        TAX
695
                                                            -- LOOK UP THE NEXT TWO DIGITS IN THE TABLE.
696
      022C
             D6 03 28
                                                TABLE, X
                                        LDA
697
      022F
             B7 1A
                                                HUNDRD --
                                        STA
698
699
      0231
             81
                                NOMO
                                        RTS
                                ***
700
701
                                ****** SUBROUTINE TO INCREMENT THE POSITION COUNTER (DEGRES). ******
702
703
                                ***
704
                                **** FIRST CHECK TO SEE IF THE BINARY COUNTER HAS REACHED A MODULO 32
705
                                ****
                                         NUMBER.
                                ****
706
707
      0232
             0D 20 04
                                INCPOS
                                       BRCLR
                                                MOD 32, STAT, INC7 'MOD 32, STAT' SET ?
708
                                ***
709
      0235
             A6 08
                                        LDA
                                                #8
710
      0237
             20 02
                                        BRA
                                                INC
                                                                INCREMENT THE POSITION BY 0.008 DEGREES.
711
712
      0239
             A6 07
                                INC7
                                        LDA
                                                #7
                                                                      NO ....
713
      023B
             B7 1D
                               INC
                                        STA
                                                POSINC
                                                                INCREMENT THE POSITION BY 0.007 DEGREES.
714
                                ***
715
                                **** ROUTINE TO INCREMENT THE POSITION COUNTER ,'DEGREES', BY A
716
                               ***
                                        PREDETERMINED AMOUNT, 'POSINC'.
717
                                ****
718
      0230
             B6 14
                                        LDA
                                                PTR1
719
      023F
             BB 1D
                                        ADD
                                                POSINC
720
      0241
             A1 09
                                        CMP
                                                         PTR1 > 9 ?
                                                #9
721
      0243
             23 05
                                        BLS
                                                OK3
                                                         NO, WE'RE OK HERE. LOOK UP THE FIRST DIGIT.
```

```
722
     0245
           AO OA
                                   SUB
                                          #10
                                                 YES ... MODIFY THE CTPTR,
                                                 SET THE CARRY, AND
723
     0247
            00
                                   SEC
     0248
          20 01
724
                                   BRA
                                          OK3A
                                                 USE TABLE LOOK UP.
725
                           OK3
726
     024A
           98
                                   CLC
                                                        NO CARRY EXISTS IF WE ENTER AT THIS POINT.
     024B
          B7 14
727
                           OK3A
                                   STA
                                          PTR1 --
728
     0240
          97
                                  TAX
                                                   -- LOOK UP THE LEAST SIGNIFICANT DIGIT.
729
     024E
           D6 03 28
                                   LDA
                                          TABLE,X --
730
731
     0251
          B7 19
                                   STA
                                          THOUTH --
     0253
           24 24
                                   BCC
                                          DONE
732
                                                      AND CONTINUE ONLY IF THERE WAS A CARRY.
                           ****
733
                           ****
734
     0255
           B6 13
                                          PTR2
735
                                   LDA
     0257
          A9 00
                                   ADC
                                          #0
                                                 ADD THE CARRY.
736
                                   CMP
                                          #99
737
     0259
          A1 63
                                                 PTR2 > 99 ?
738
    025B
          23 05
                                   BLS
                                          OK4
                                                 NO, WE'RE OK HERE. LOOK UP THE NEXT TWO DIGITS.
                                          #100
                                                 YES ... MODIFY THE CTPTR,
739
     025D
           A0 64
                                   SUB
740
     025 F
            99
                                   SEC
                                                 SET THE CARRY,
                                                 AND USE TABLE LOOK UP.
741
     0260
          20 01
                                   BRA
                                          OK4A
                           ****
742
                                   CLC
                           OK4
743
     0262
          98
                                                        NO CARRY EXISTS IF WE ENTER AT THIS POINT.
                                          PTR2 --
744
     0263
           B7 13
                           OK4A
                                   STA
745
     0265
           97
                                   TAX
746
                                                     -- LOOK UP THE NEXT TWO DIGITS IN THE TABLE.
747
     0266
           D6 03 28
                                          TABLE,X --
                                   LDA
748
     0269
          B7 18
                                  STA
                                          HUNDTH --
749
     026B
          24 OC
                                   BCC
                                          DONE
                                                       AND CONTINUE ONLY IF THERE WAS A CARRY.
                           ****
750
                           ****
751
                                          PTR3
     0260
           B6 12
                                   LDA
752
    026F
           A9 00
                                   ADC
                                          #0 ADD THE CARRY.
753
754
    0271
           B7 12
                                   STA
                                          PTR3
     0273
755
           97
                                  TAX
                                                  -- LOOK UP THE NEXT TWO DIGITS IN THE TABLE.
                           ****
756
                                        TABLE,X --
     0274
757
            D6 03 28
                                   LDA
                                   STA ONEDEG --
           B7 17
758
    0277
                           ****
759
    0279
                           DONE
760
           81
                                   RTS
                           ***
761
                           **
762
                           ********************************
763
                           ******* SUBROUTINE TO DECREMENT THE BCD COUNTER (BCDCT). **********
764
765
          B6 16
                           SUBBCD LDA
766
    027A
                                          CTPTR1
          A0 01
                                               CTPTR > 99 ?
767
     027C
                                   SUB
                                          #1
768
     027E
           24 03
                                   BCC
                                          OK6
                                                 NO, WE'RE OK HERE. LOOK UP THE FIRST TWO DIGITS.
769
     0280
                                   ADD
                                          #100
                                                 YES, MODIFY THE CTPTR, AND
           AB 64
                                                  GENERATE A BORROW.
770
     0282
           99
                                   SEC
                           ***
771
     0283
           B7 16
772
                           OK6
                                   STA
                                          CTPTR1 --
     0285
           97
773
                                   TAX
774
                                                    -- LOOK UP THE TWO LEAST SIGNIFICANT DIGITS.
     0286
           D6 03 28
775
                                   LDA
                                          TABLE, X --
     0289
           B7 1B
                                          TENONE --
776
                                  STA
777
     028B
          24 OC
                                   BCC
                                          COMPLT
                                                     AND CONTINUE ONLY IF THERE WAS A BORROW.
                           ***
778
                           ***
779
                                          CTPTR2
780
     0280
           B6 15
                                   LDA
781
     028F
           A2 00
                                   SBC
                                          #0 SUBTRACT THE CARRY. CTPTR > 99 ?
     0291
           B7 15
                                          CTPTR2 --
782
                                   STA
783
     0293
           97
                                   TAX
                                                   -- LOOK UP THE NEXT TWO DIGITS IN THE TABLE.
784
                                          TABLE,X --
     0294
785
          D6 03 28
                                   LDA
     0297 B7 1A
786
                                   STA
                                          HUNDRD --
787
```

```
788
     0299 81
                             COMPLT RTS
                             ***
789
790
                             ****** SUBROUTINE TO DECREMENT THE POSITION COUNTER (DEGRES). *******
791
                             ***
792
                             **** FIRST CHECK TO SEE IF THE BINARY COUNTER HAS REACHED A MODULO 32
793
794
                             ****
                                      NUMBER.
                             ****
795
796
     029A
            00 20 04
                             DECPOS BRCLR
                                             MOD 32, STAT, DEC7
                                                                   'MOD_32,STAT' SET ?
                             ****
797
     0290
            A6 08
798
                                     LDA
                                             #R
                                                                     YES ...
     029F
            20 02
                                     BRA
                                             DEC
                                                            DECREMENT THE POSITION BY 0.008 DEGREES.
799
                             ****
800
            A6 07
                             DEC7
                                     LDA
                                             #7
801
     02A1
                                             POSINC DECREMENT THE POSITION BY 0.007 DEGREES.
            B7 10
802
     02A3
                             DEC
                                     STA
                             ***
803
                             **** ROUTINE TO DECREMENT THE POSITION COUNTER ,'DEGREES', BY A
804
                             ***
                                     PREDETERMINED AMOUNT, 'POSINC'.
805
                             ***
806
807
     02A5
            B6 14
                                     LDA
                                             PTR1
808
     02A7
            BO 10
                                     SUB
                                             POSINC PTR1 < 0 ?
                                                     NO, WE'RE OK HERE. LOOK UP THE FIRST DIGIT.
809
     02A9
            24 03
                                     BCC
                                             OK8
810
     02AB
            AB OA
                                     ADD
                                             #10
                                                     YES, MODIFY THE CTPTR, AND
            99
                                     SEC
                                                     GENERATE A BORROW.
811
     02AD
812
     02AE
            B7 14
                             OK8
                                     STA
                                             DTP1
813
            97
     02B0
814
                                     TAX
815
                                                        -- LOOK UP THE LEAST SIGNIFICANT DIGIT.
     02B1
            D6 03 28
                                     LDA
                                             TABLE,X
816
817
     02B4
            B7 19
                                     STA
                                             THOUTH --
            24 1F
                                             DUNSUB
                                                       AND CONTINUE ONLY IF THERE WAS A BORROW.
     02B6
                                     BCC
818
819
820
821
     0288
            B6 13
                                     LDA
                                             PTR2
822
     02BA
           A2 00
                                     SBC
                                             #0
                                                     SUBTRACT THE BORROW. PTR2 < 0 ?
                                                     NO, WE'RE OK HERE. LOOK UP THE NEXT TWO DIGITS.
823
            24 03
                                             OK9
     02BC
                                     BCC
824
     02BE
            AB 64
                                     ADD
                                             #100
                                                     YES, MODIFY THE CTPTR, AND
            99
825
     02C0
                                     SEC
                                                     GENERATE A BORROW.
826
     02C1
            B7 13
827
                             OK9
                                     STA
                                             PTR2
828
     02C3
            97
                                     TAX
                                                        -- LOOK UP THE NEXT TWO DIGITS IN THE TABLE.
829
830
     02C4
            D6 03 28
                                     LDA
                                             TABLE,X --
            B7 18
                                             HUNDTH --
831
     02C7
                                     STA
            24 OC
     0209
832
                                     BCC
                                             DUNSUB
                                                         AND CONTINUE ONLY IF THERE WAS A CARRY.
                             ***
833
834
                             ***
835
     02CB
            B6 12
                                             PTR3
                                     LDA
836
            A2 00
     02CD
                                     SBC
                                                     SUBTRACT THE BORROW.
                                             #0
     02CF
            B7 12
                                     STA
837
                                             PTR3
838
     02D1
            97
                                     TAX
839
                                                         -- LOOK UP THE NEXT TWO DIGITS IN THE TABLE.
840
     0202
            D6 03 28
                                     LDA
                                             TABLE,X --
841
     0205
            B7 17
                                     STA
                                             ONEDEG --
                             ****
842
843
     0207
            81
                             DUNSUB
                                     RTS
844
                             ***
845
                             **
846
                             **
847
                             *************************************
848
849
                             ** OUTPUT COUNT (OUTCT). SUBROUTINE TO MOVE THE CURRENT COUNT (BCDCT)
850
                             **
                                      TO THE OUTPUT PORTS. REMOVES THE DECIMAL POINT FROM THE
851
                             **
                                      DISPLAY AND BLANKS ALL BUT THE LEAST SIGNIFICANT DIGIT. ALSO
852
                             **
                                      SETS THE MINUS SIGN IF APPROPRIATE.
                             ++
```

853

```
854
              0208
                               OUTCT
                                        EQU
855
856
      0208
              B6 1B
                                        LDA
                                                TENONE
             B7 02
857
      02DA
                                        STA
                                                PORTC
                                **
858
859
      02DC
              B6 1A
                                        LDA
                                                HUNDRD
860
      02DE
             B7 00
                                        STA
                                                PORTA
861
862
      02F0
              1E 01
                                        BSFT
                                                DECPT, PORTB
863
      02E2
             19 01
                                        BCLR
                                                BLANK, PORTB
864
865
      02E4
             81
866
                               ***
867
868
                               **
869
                                ** OUTPUT POSITION (OUTPOS). SUBROUTINE TO MOVE THE CURRENT POSITION
                               **
                                         COUNT (BCDCT) TO THE OUTPUT PORTS. THE DECIMAL POINT IS
870
                               **
871
                                         DISPLAYED , AND ONLY THE MOST SIGNIFICANT DIGIT IS BLANKED.
872
                                **
873
              02E5
                               OUTPOS EQU
874
875
      02E5
             B6 19
                                        LDA
                                                THOUTH
876
      02E7
             A1 05
                                        CMP
                                                #5
             25 2D
                                                TRUNC
                                                                  IF 5 > 'THOUTH' SIMPLY TRUNCATE THE
877
      02E9
                                        BLO
                                                               -- DISPLAY. OTHERWISE...
             B6 18
                                        LDA
                                                HUNDTH
878
      02EB
                                                               -- IF THE LAST DIGIT ISN'T A NINE IT IS
879
      02ED
             A4 09
                                        AND
                                                #9
             A1 09
880
                                                #9
                                                               -- EASY TO ROUND UP. JUST ADD A ONE.
      02EF
                                        CMP
881
      02F1
             26 1D
                                                DECIMAL
                                                               --
                                        BNE
882
      02F3
                                                HUNDTH
                                                               -- BUT IF THE LAST DIGIT IS A NINE CHECK TO
             B6 18
                                        LDA
883
      02F5
             A1 99
                                                #$99
                                                               -- SEE IF IT'S 99. IF SO IT GETS GRIM.
                                        CMP
884
             27 04
                                                UGLY
      02F7
                                        BEQ
885
      02F9
             AB 07
                                        ADD
                                                #7
                                                               -- IF THE NUMBER IS X9 AND X .NE. 9, THEN
886
             20 1D
                                                PCOUT
                                                               -- JUST ADD SEVEN TO ROUND UP. DUE TO
      02FB
                                        BRA
                               **
887
                                                               -- HEXIDECIMAL.
                               **
888
                                                               -- IF THE LOW TWO DIGITS ARE BOTH NINES
             A6 00
889
                                                #00
                                                                AND WE NEED TO ROUND UP....
      02FD
                               UGLY
                                        LDA
             B7 02
890
      02FF
                                                PORTC
                                                                  MAKE THE LOW TWO DIGITS BOTH ZEROS
                                        STA
                                                                  AND SET THE CARRY.
891
      0301
             99
                                        SEC
892
893
      0302
             B6 17
                                        LDA
                                                ONEDEG
                                                                  CHECK THE LAST DIGIT AS BEFORE.
894
      0304
             A4 09
                                                                  IF USING THIS PORTION OF THE CODE
                                        AND
                                                #9
             A1 09
895
      0306
                                        CMP
                                                #9
                                                                 THERE HAD TO BE A CARRY.
896
      0308
             26 13
                                        RNF
                                                NEXT
                                                             -- IF THE LAST DIGIT IS A NINE DO THE
897
      030A
             B6 17
                                        LDA
                                                ONEDEG
                                                                  CARRY HERE. IF NOT USE THE ADC
898
      030C
             AB 07
                                        ADD
                                                #7
                                                                  INSTRUCTION TO TAKE CARE OF IT
899
             20 11
                                                PAOUT
      030E
                                        BRA
                                                                  BELOW.
900
      0310
             B6 18
                                DECIMAL LDA
                                                HUNDTH --
901
      0312
             AB 01
                                        ADD
                                                #1
902
                                                             -- THIS IS ALL THAT NEEDS TO BE DONE IF
903
      0314
             B7 02
                                                PORTC
                                                                  THE LAST DIGIT IS NOT A NINE.
                                        STA
904
      0316
             20 05
                                        BRA
                                                NEXT
905
                                ++
906
      0318
             B6 18
                                TRUNC
                                        LDA
                                                HUNDTH
907
      031A
             B7 02
                               PCOUT
                                        STA
                                                PORTC
                                                          -- AND IF THERE IS NO CARRY IT'S EVEN EASIER.
908
             98
      031C
                                        CLC
909
             B6 17
                                                ONEDEG
910
      031D
                               NEXT
                                        LDA
911
      031F
             A9 00
                                        ADC
                                                #0
912
      0321
             B7 00
                               PAOUT
                                                PORTA
                                        STA
913
                                **
      0323
              18 01
914
                                        BSET
                                                BLANK, PORTB
915
      0325
             1F 01
                                        BCLR
                                                DECPT, PORTB
916
917
      0327
             81
                                        RTS
918
                                **
919
```

```
920
921
                              ** SET UP THE TABLE TO BE USED WITH BCD INCREMENT/DECREMENT ROUTINES.
922
923
                                      ENDS
924
                                      DATA
      0328
             00 01 02 03 04
                                             $00,$01,$02,$03,$04,$05,$06,$07,$08,$09
925
                              TABLE
                                      FCB
             05 06 07 08 09
      0320
926
      0332
             10 11 12 13 14
                                      FCB
                                             $10,$11,$12,$13,$14,$15,$16,$17,$18,$19
             15 16 17 18 19
      0337
927
      033C
             20 21 22 23 24
                                      FCB
                                             $20,$21,$22,$23,$24,$25,$26,$27,$28,$29
      0341
             25 26 27 28 29
928
      0346
             30 31 32 33 34
                                      FCB
                                             $30,$31,$32,$33,$34,$35,$36,$37,$38,$39
             35 36 37 38 39
      034B
929
      0350
             40 41 42 43 44
                                      FCB
                                             $40,$41,$42,$43,$44,$45,$46,$47,$48,$49
      0355
             45 46 47 48 49
930
             50 51 52 53 54
      035A
                                      FCB
                                             $50,$51,$52,$53,$54,$55,$56,$57,$58,$59
      035F
             55 56 57 58 59
931
      0364
             60 61 62 63 64
                                      FCB
                                             $60,$61,$62,$63,$64,$65,$66,$67,$68,$69
             65 66 67 68 69
      0369
932
      036E
             70 71 72 73 74
                                      FCB
                                             $70,$71,$72,$73,$74,$75,$76,$77,$78,$79
             75 76 77 78 79
      0373
933
      0378
             80 81 82 83 84
                                      FCB
                                             $80,$81,$82,$83,$84,$85,$86,$87,$88,$89
      0370
            85 86 87 88 89
934
      0382
            90 91 92 93 94
                                      FCB
                                             $90,$91,$92,$93,$94,$95,$96,$97,$98,$99
            95 96 97 98 99
      0387
935
                                      ENDS
                              *
936
                                      CODE
937
                              ***
                                     *****************************
938
                              **
939
                              **
                                                     SET UP MASK OPTION REGISTER.
940
                              **
941
     038C
                                     ABSOLUTE
                                                     JUST TO ENSURE THAT THE INTERRUPT VECTORS
                              **
942
                                                     ARE CORECTLY LOCATED.
943
                              **
944
                              **
945
     0F38
                                      ORG
                                             MOR
946
     0F38
            07
                                             #BIT2+BIT1+BIT0
                                      FCB
947
948
                              **
                                     COMMENTS:
949
                              **
                                     BIT 7
                                             CLOCK SOURCE 0 = CRYSTAL.
                             **
950
                                     BIT 6
                                             TIMER OPTION 0 = INTERNAL.
                             **
951
                                     BIT 5
                                             TIMER/CLOCK SOURCE 0 = INTERNAL.
                             **
952
                                     BIT 4
                                             NOT USED.
                             **
953
                                     BIT 3
                                             NOT USED.
954
                             **
                                     BIT 2
                                             SET
955
                             **
                                     BIT 1
                                             SET
                                                  - PRESCALE SELECT 111 => 128
                             **
956
                                     BIT 0
                                             SET -
                             **
957
958
                             **
959
                             ************
960
                             **
961
                             **
                                                      ASSIGN INTERRUPT VECTORS.
962
                             **
963
     OFF8
                                     ORG
                                             INTRPT
964
                             **
     OFF8
965
            0139
                                     FDB
                                             BLINK
                                                     TIMER/INT2 INTERRUPT VECTOR.
966
     OFFA
            0158
                                             COUNT
                                     FDB
                                                     EXTERNAL INTERRUPT VECTOR.
967
     OFFC
            0158
                                     FDR
                                             COUNT
                                                     SOFTWARE INTERRUPT VECTOR, NOT USED.
968
     OFFE
            0080
                                     FDB
                                             RESTRT RESET VECTOR.
969
970
                             **
971
                             **
972
                                     ENDS
973
     1000
                                     END
```

Lines Assembled: 973 Assembly Errors: 0

LIST OF REFERENCES

- 1. Ayers, Gary Robert, Calibration and Initialization of the NPS Modified Infrared Search and Target Designation (IRSTD) System, Master's Thesis, Naval Postgraduate School, Monterey, CA, December 1987.
- 2. Norton, Harry N., Sensor and Analyzer Handbook, Prentice Hall Inc., 1982.
- 3. Herceg, Edward E., Handbook of Measurement and Control, Schaevitz Engineering, 1972.
- 4. Lenk, John D., Handbook of Controls and Instrumentation, Prentice Hall Inc., 1980.
- 5. Farrand Controls, INDUCTOSYN Precision Linear and Rotary Position Transducers, pp. 2-6, undated.
- 6. Doebelin, Ernest O., Measurement Systems, Application and Design, Mc Graw-Hill Book Co., 1976.
- 7. Hewlett Packard, Application Note 1011, Design and Operational Considerations for the HEDS-5000 and HEDS-6000 Incremental Optical Shaft Encoders, undated.
- 8. Installation and Operation Manual, PT1250DC Heavy Duty Pan/Tilt, p. 12, PELCO Sales Co., 1988.
- 9. Hewlett Packard, 56 mm Diameter Two and Three Channel Incremental Optical Encoder Kit, Technical Data, January 1984.
- 10. Motorola Semiconductors, MC68705U3 Advance Information, Motorola Inc., 1981.
- 11. National Semiconductor Corporation, Logic Databook, Vol. 2, 1984.

- 12. Terman, F.W., Latches and Flip Flops, Lab Notes for EC2820 (Digital Circuits), pp. 3,4, Naval Postgraduate School, undated.
- 13. Taub, Herbert, Digital Circuits and Microprocessors, pp. 130-135, McGraw-Hill Book Co., 1982.
- 14. Motorola, M6805 HMOS, M146805 CMOS Family, Microcomputer/Microprocessor User's Manual, 2nd ed., Prentice-Hall Inc., 1983.
- 15. Installation and Operation Manual, Motorized Zoom Lenses, p. 6, PELCO Sales Co., undated.
- 16. National Semiconductor Corporation, Linear Databook, pp. (1-181)-(1-183), 1982.
- 17. 2500 A.D. Software, 6805 Macro Assembler, Version 4.02, pp. (1-1)-(2-38), undated.
- 18. Motorola, M68705EVM Evaluation Module User's Manual (M68705EVM; AD4), 4th ed., Motorola Inc., 1987.
- 19. Houghton, P.S., Gears; Spur, Helical, Bevel, Internal, Epicyclic, and Worm, 3rd ed., pp. 1.4,1.5, Technical Press, 1970.
- 20. Peebles. Peyton Z., Jr., Probability, Random Variables, and Random Signals, pp. 121-122, 2nd ed., McGraw-Hill Book Co., 1987.
- 21. Lloyd, Scot D., An Autopilot Design for the United States Marine Corps' Airborne Remotely Operated Device, Master's Thesis, Naval Postgraduate School, Monterey, CA, September 1987.

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